Integration of Nanoscale Structures with Electronics

Philip Leong,

The University of Sydney
http://www.ee.usyd.edu.au/people/philip.leong/talks.html

THE UNIVERSITY OF SYDNEY

Computer Engineering Laboratory

- Focuses on how to use parallelism to solve demanding problems
  - Novel architectures, applications and design techniques using VLSI, FPGA and parallel computing technology
- Research
  - Reconfigurable computing
  - Nanoscale interfaces
  - Machine learning
- **Lab**
  - 4 postdoctoral researchers
  - 8 PhD, 2 Masters students

Accelerator Project

- Project aims to develop capabilities in the integration of nanotechnology with electronic integrated circuits through three subprojects
  1. Photonics - electrical interface to photonic signal processing chip
  2. LowT - analog transistor array for characterizing low-temperature devices
  3. Sensor – graphene based sensor

- Collaborations Ben Eggleton, Michael Biercuk, Stefano Palomba
  - One Postdoc (Mostafa Rahimi Azghadi)
  - Endeavour Fellow (Yee Hui Lee)
  - PhD students (Andri Mahendra, Cong Ngyuen Dao, Xiang Zhang)
  - Undergraduates (Ed Brackenreg)

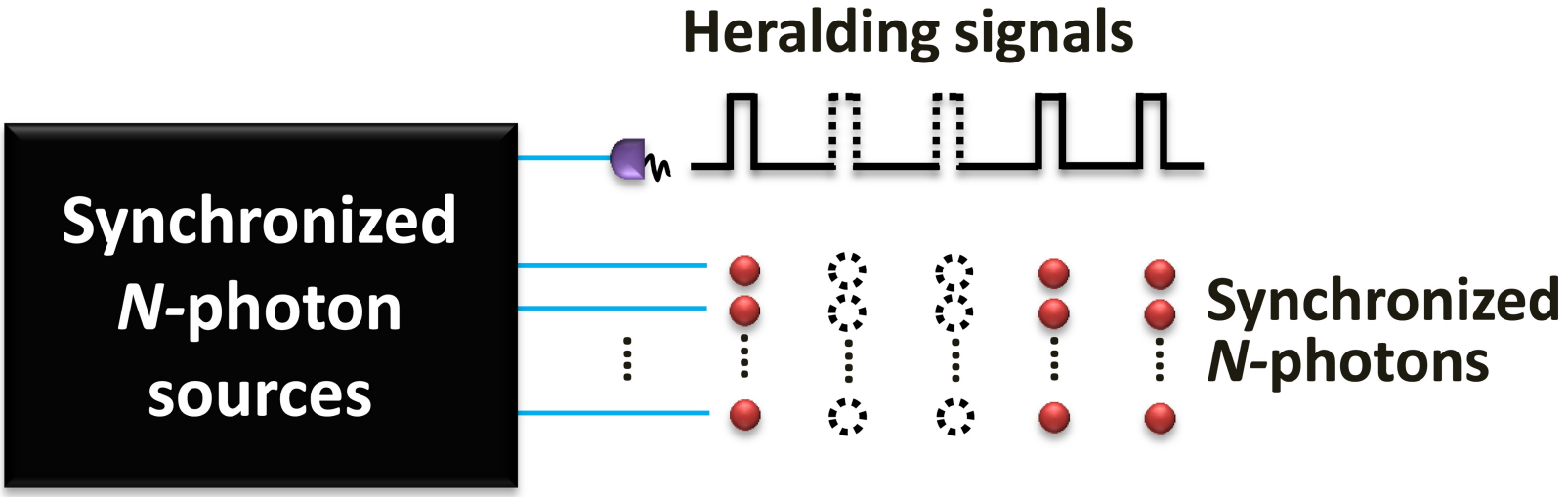
Photonics

Motivation

- Efficient generation of single-photons is holding back quantum photonics
- Actually we don’t want single-photons, we want multi-photons

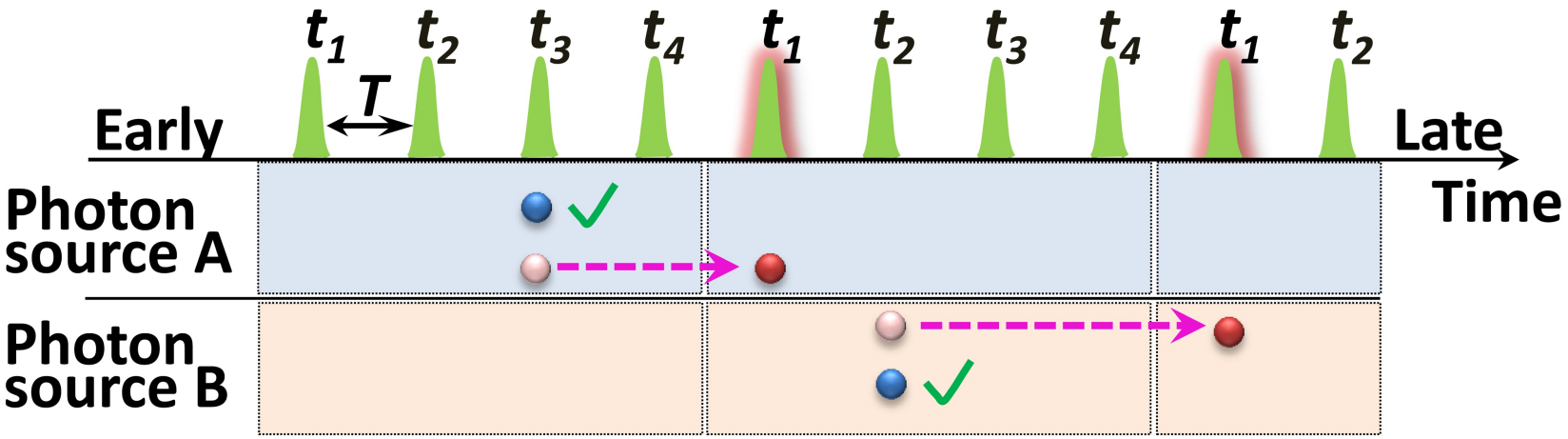
Photon pair generation

- Probability of photon-photon interaction decreases exponentially with number of single photons
- Previous work: generation of single photons
- Aim – generate synchronised photon pairs with electronic heralding signal



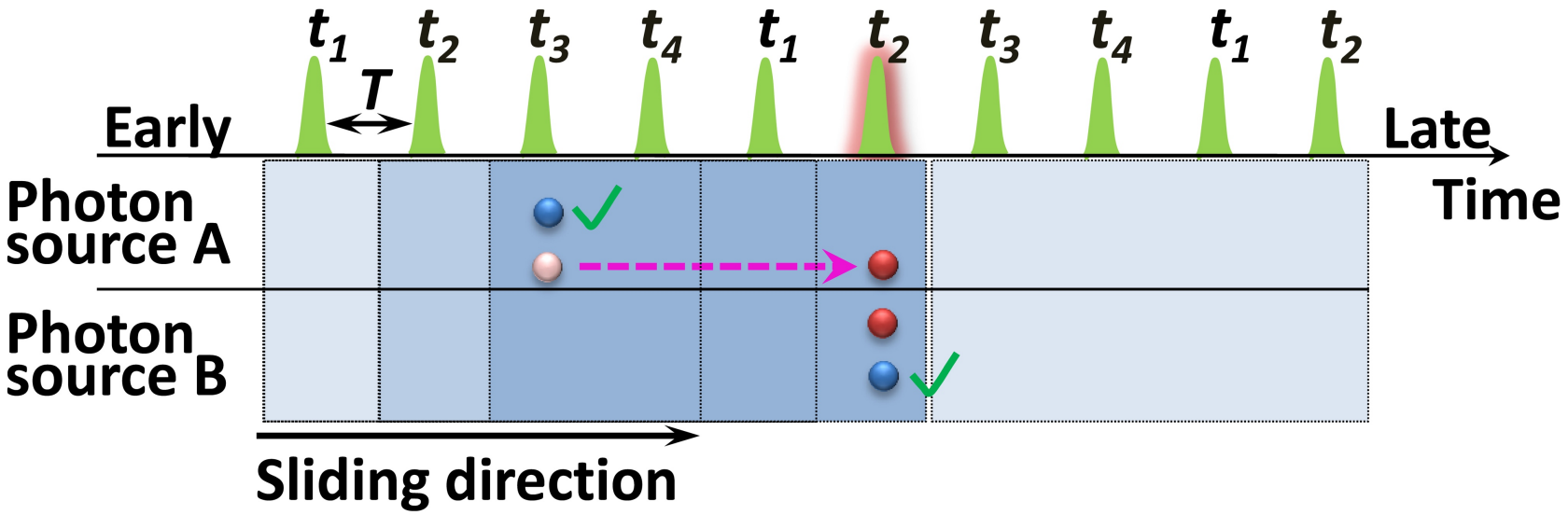
Independent Temporal Multiplexing (ITM)

› For single photon pairs, can detect one and delay the other so it always appears at t1



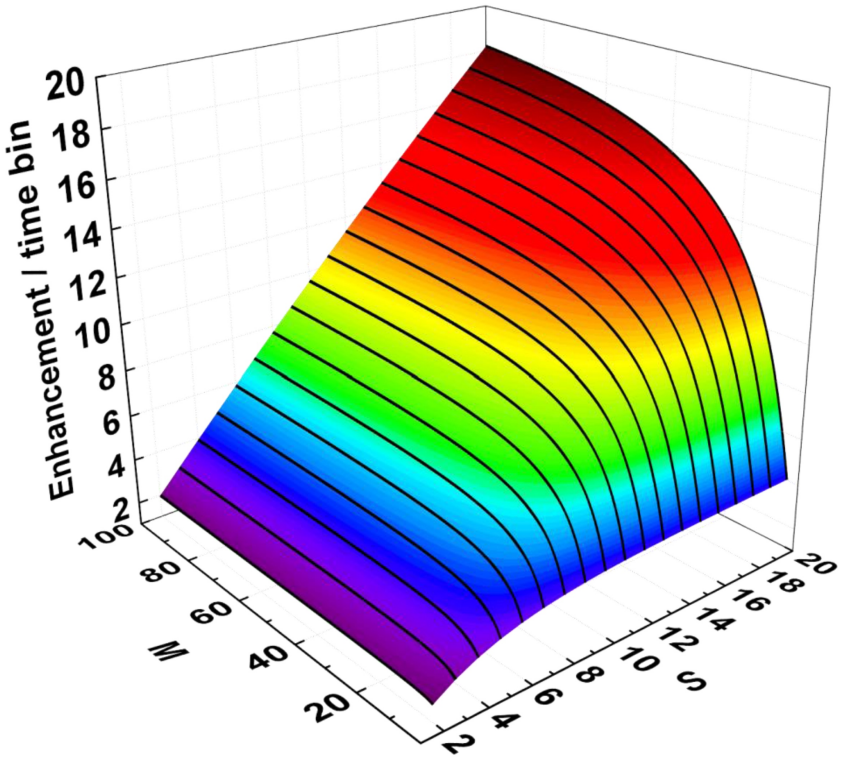
Relative Temporal Multiplexing (RTM)

- If photons appear within a certain window can generate pairs
  - Detect occurrence of a top and bottom photon and delay appropriately
  - Increase probability pairs are generated



Efficiency of relative temporal multiplexing

- M is the number of time bins per window
- S is the number of photon sources
- The better resolution (M) and more photon sources (S), the higher the enhancement
  - Unfortunately, losses are introduced

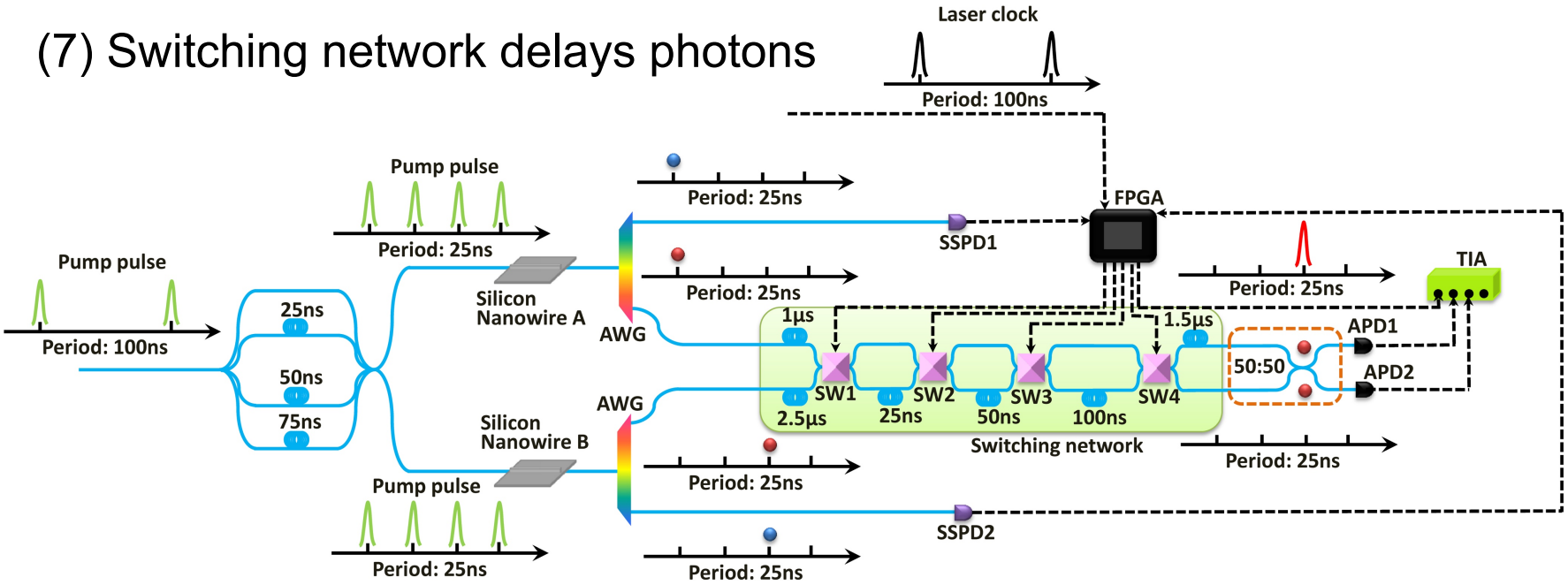


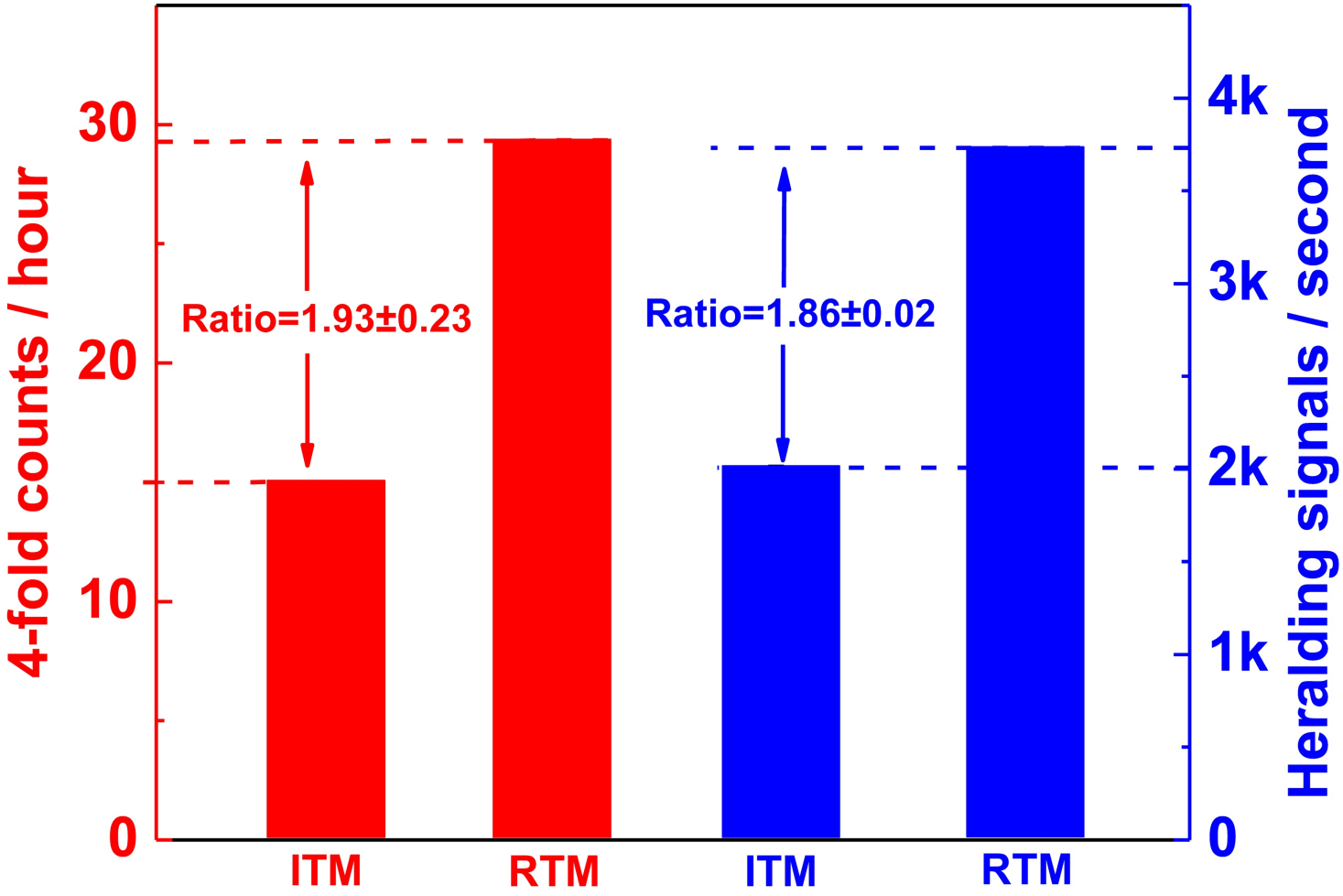
Experimental Setup

(1) Pump laser at 100 ns (2) Period reduced to 25 ns (3) Two nanowires generate photon pairs; (4) AWG separate photon pairs (5) Heralding photons detected by SSPD

(6) FPGA generates appropriate signals

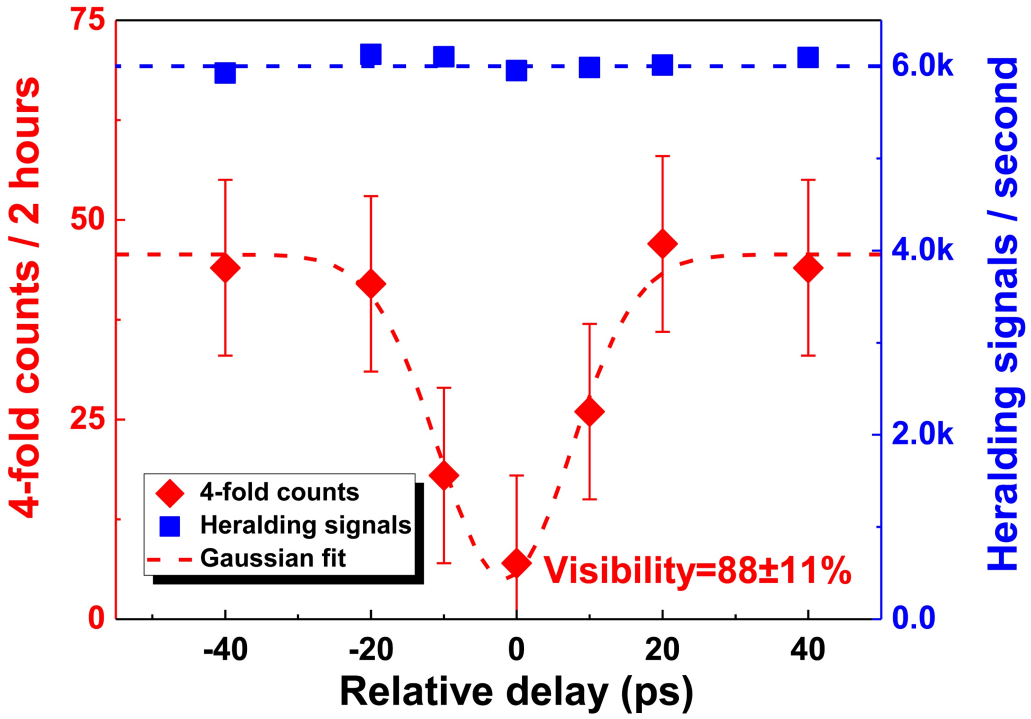
(7) Switching network delays photons




4-fold counts / hour
30
20
10
0
Ratio=1.93±0.23
Ratio=1.86±0.02
4k
3k
2k
1k
0
Heralding signals / second
ITM
RTM
ITM
RTM

Results

- Hong-Ou-Mandel quantum interference
- Red is 4-fold counts after subtracting noise
- Visibility > 50% demonstrates non-classical effect



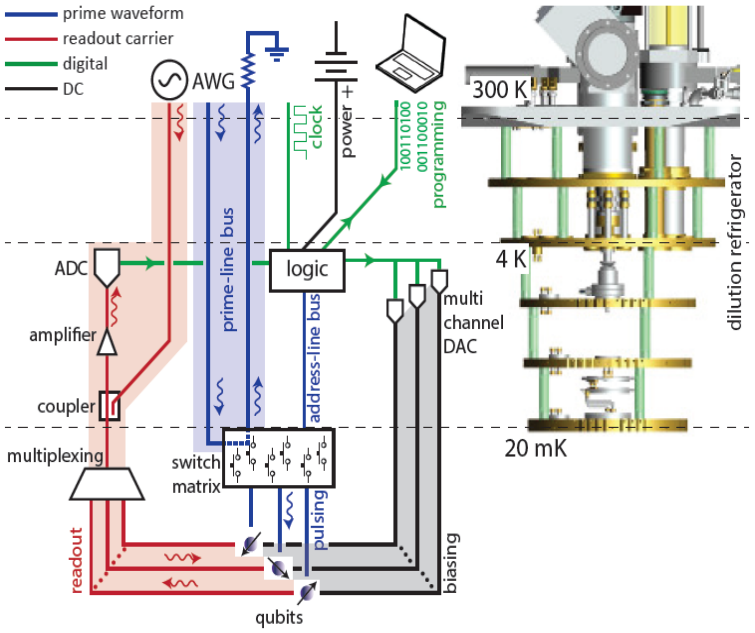
Summary

- Demonstrated we can generate indistinguishable photon pairs
- Enhancement increases linearly with number of photon sources
- All the individual components have been demonstrated for an efficient single photon generation chip based on these techniques
  - Would be an important building block for quantum photonic systems

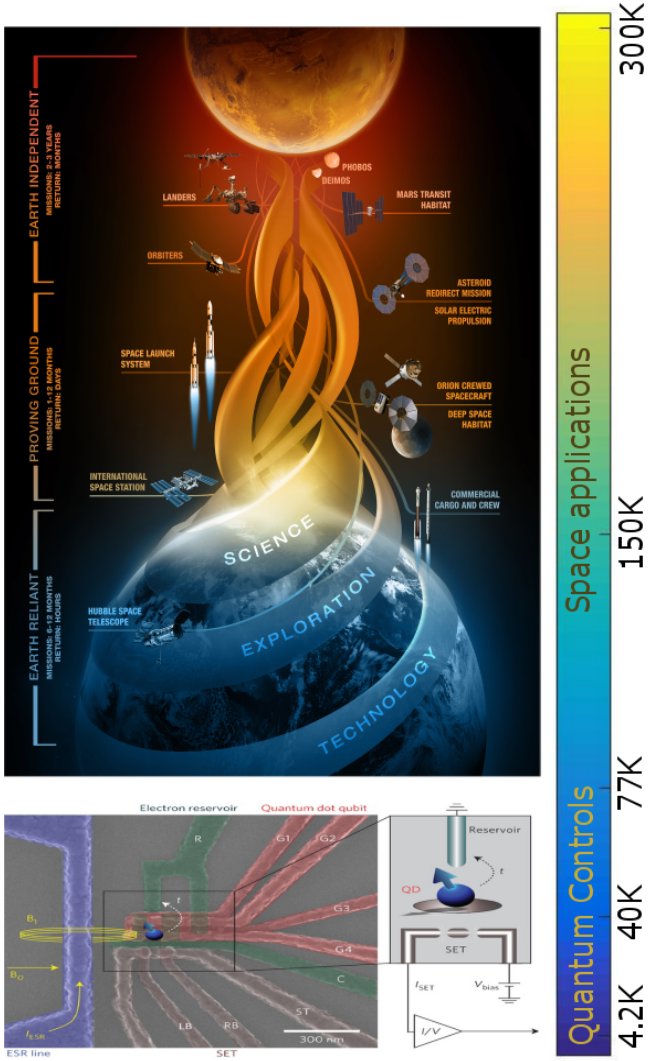
Low Temperature Electronics

Motivation

- Demand on low temperature electronic circuits
- No transistor model for circuit evaluation and circuit design at cryogenic temperatures

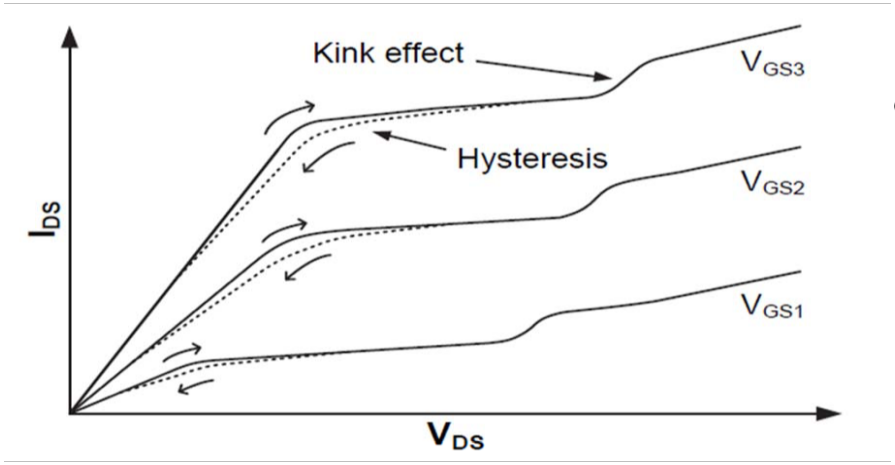


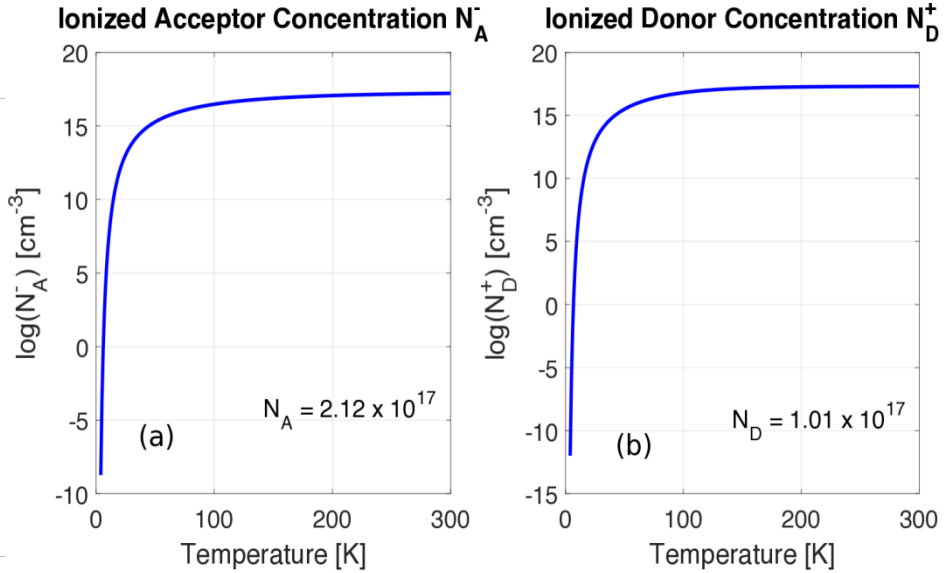
Cryogenic control architecture for large-scale quantum computing [1]



Issues:

- Freeze-out of carriers (due to incomplete ionization of the dopants)
- Kink effect and hysteresis effect
- Matching property

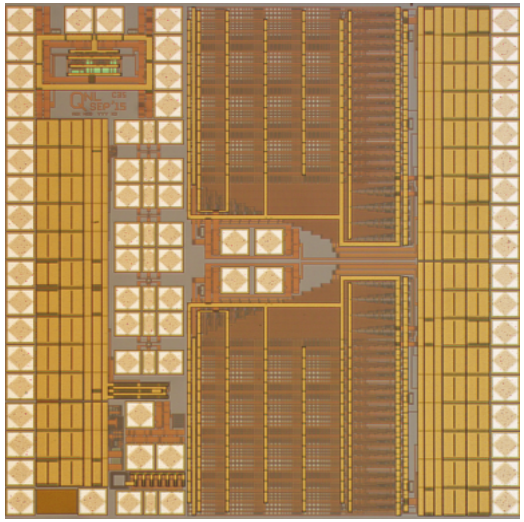


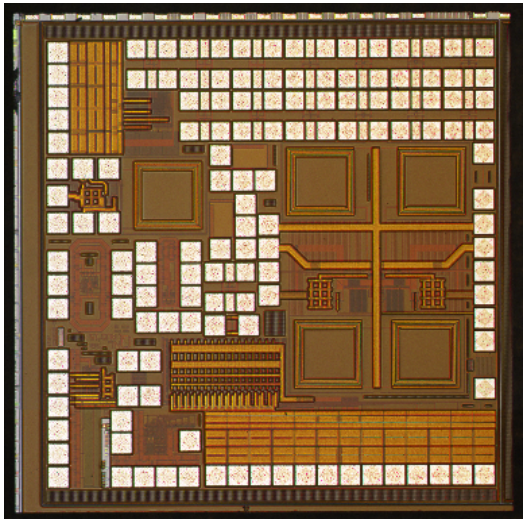


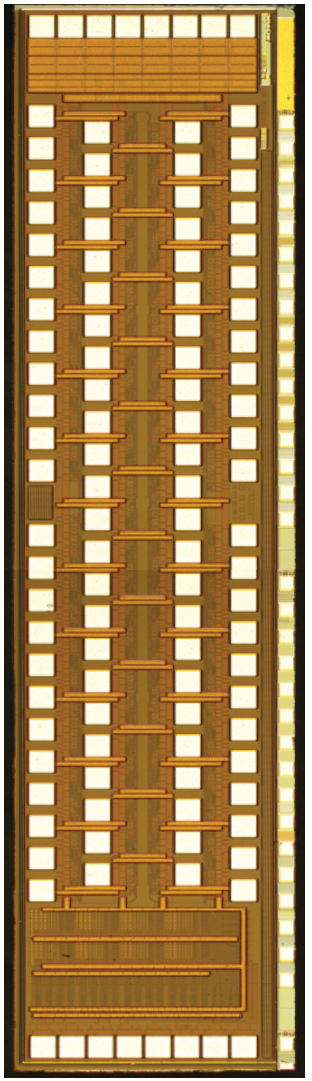
➢ **Characterize and develop transistor models (CMOS) for low temperature circuit design.**

Test chips

- Test chips were fabricated in 0.35 um AMS CMOS, BiCMOS
  - Bare transistors (PMOS, NMOS, SiGe BJT)
  - Transistor Arrays
  - Diodes, digital gates, resistors, capacitors
  - Op-Amp, ADC, DAC, Mixer, VCO …

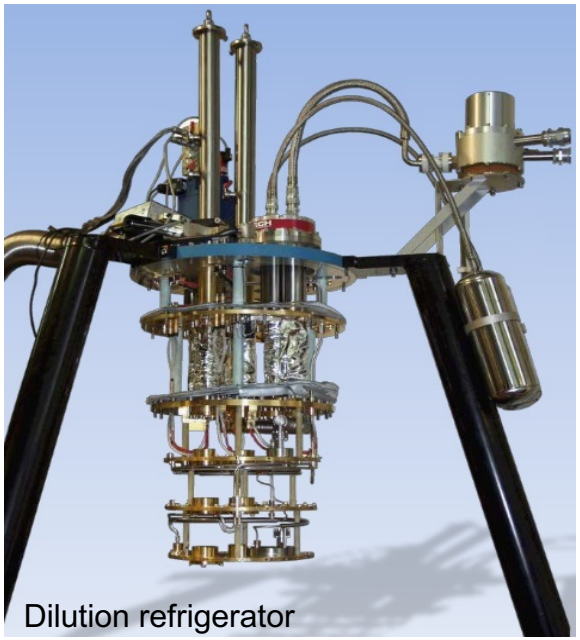


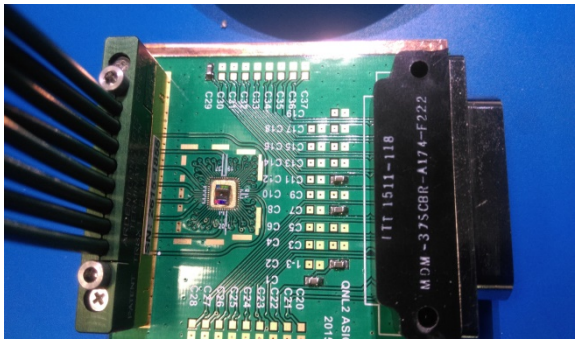


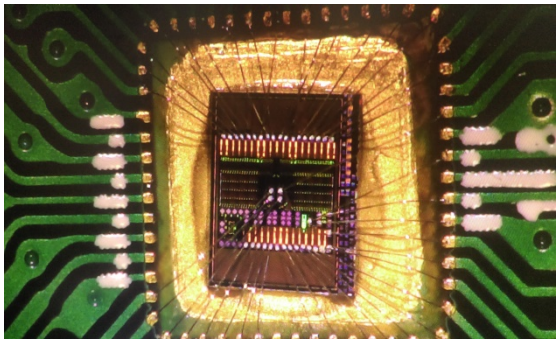


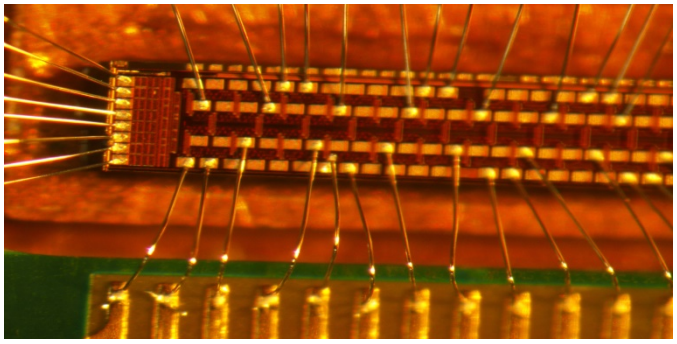
Experimental setup

- A cryogenic probe station (LakeShore CRX-4K) and a dilution refrigerator (Leiden CF450) were used.
- A semiconductor analyzer (Keysight B1500A) was used to measure I-V characteristics.


Dilution refrigerator








Probe station

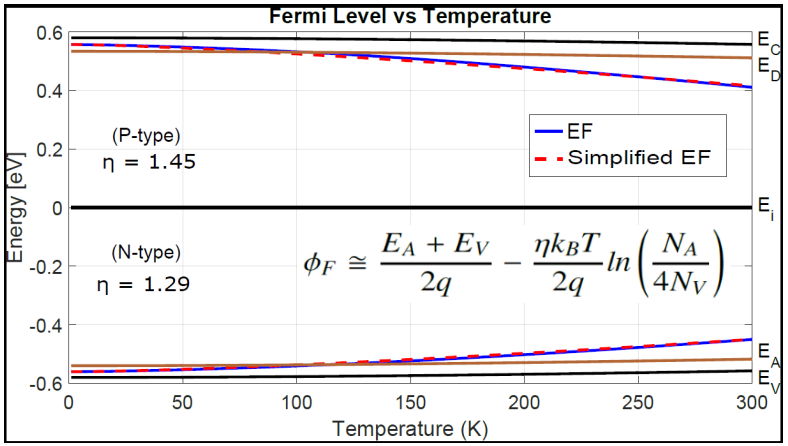
Threshold Voltage:

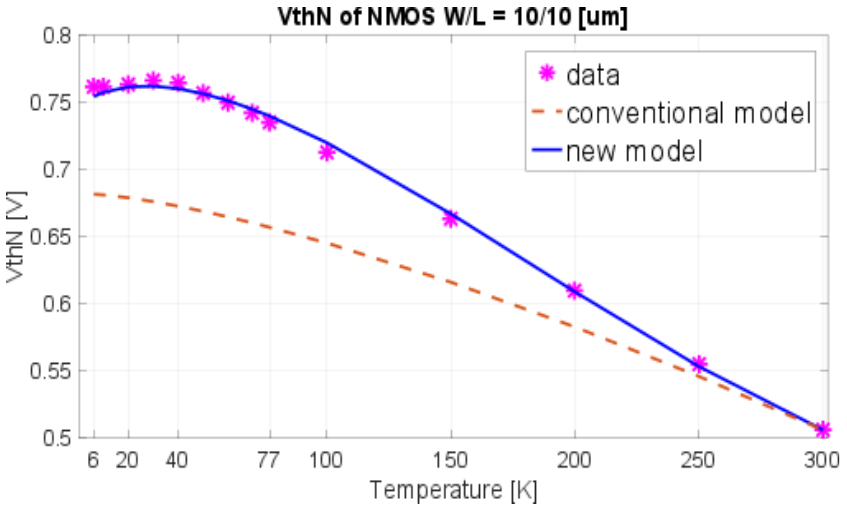
Enhanced MOSFET threshold voltage [2]:

$$V_{th0} = |\phi_F| - \phi_{gate} - \frac{Q'_o}{C'_{ox}} + \gamma\sqrt{2|\phi_F|} + \Delta V_G$$

with field-assisted ionization:

$$\Delta V_G = \frac{\varepsilon_{Si} T_{ox}}{4q}\beta^2\left(\phi_{AF0}\frac{T}{T_0} - \phi_{AF}\right)^2$$





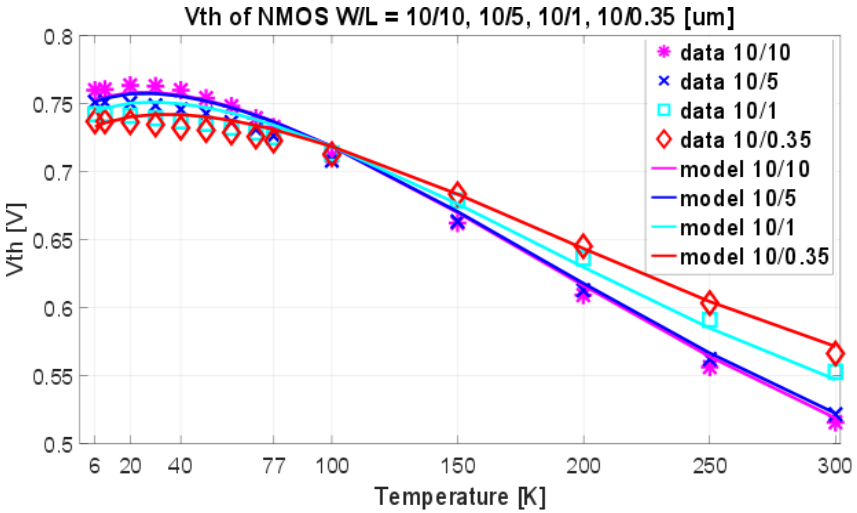
Threshold voltage:

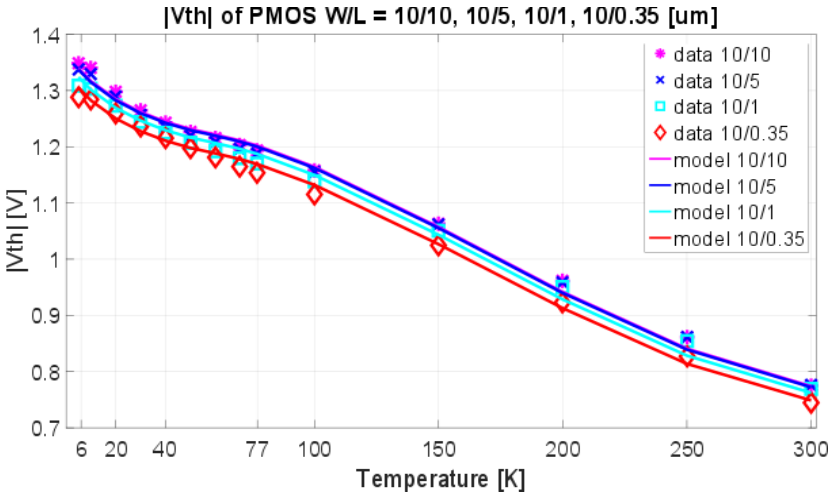
For short channel devices:

$$V_{th} = V_{th0} + \Delta Vth \times f_{SC}(T)$$

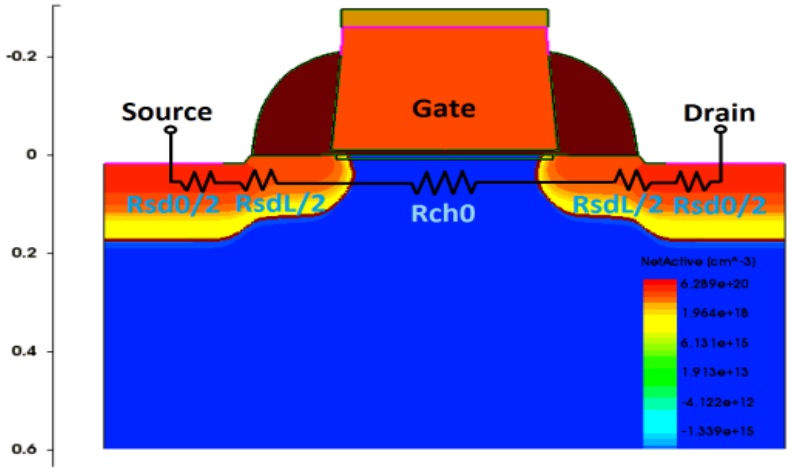
$$f_{SC}(T) = \left(1 + sgn(\phi_F(T))\frac{\phi_F(T)}{\phi_F(T_c)}\right)\delta_{Vth}$$

$$\Delta Vth = \Delta V_{LD} - \Delta V_{SC} - \Delta V_{DIBL}$$





Channel and Series Resistance:



Series resistance is assumed as [3]

$$R_{sd} = R_{sd0} + R_{sdL}$$

Total channel resistance is

$$R_{tot} = R_{ch0}L + R_{sd0} + R_{sdL}$$

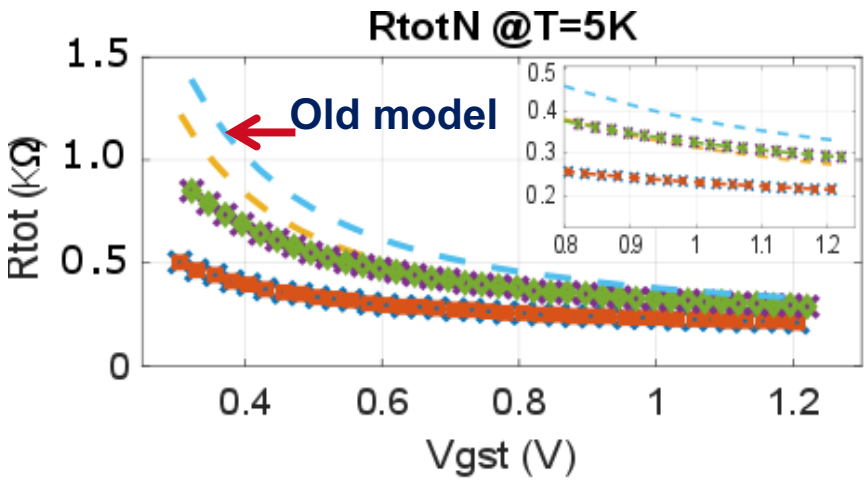
Using a set of same width devices, different length, device resistance can be extracted as

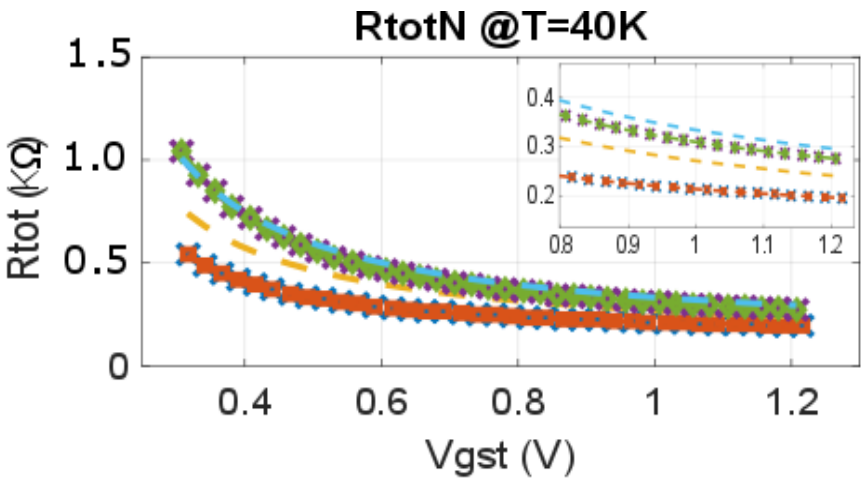
$$R_{ch0} \approx \frac{R_{tot,L_1} - R_{tot,L_2}}{L_1 - L_2}, \quad R_{sd0} \approx R_{tot,L_1} - R_{ch0}L_1.$$

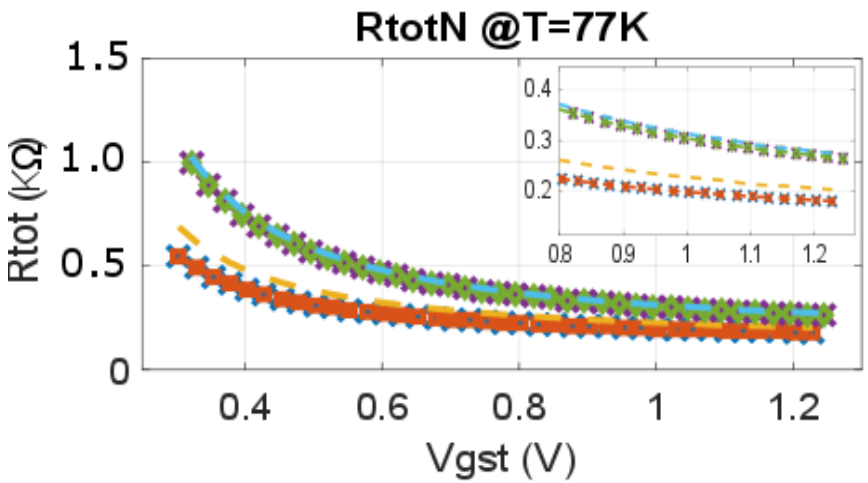
Mobility (μ_g) and its attenuation factor (θ) are extracted from the coefficients of the best fit Rch0

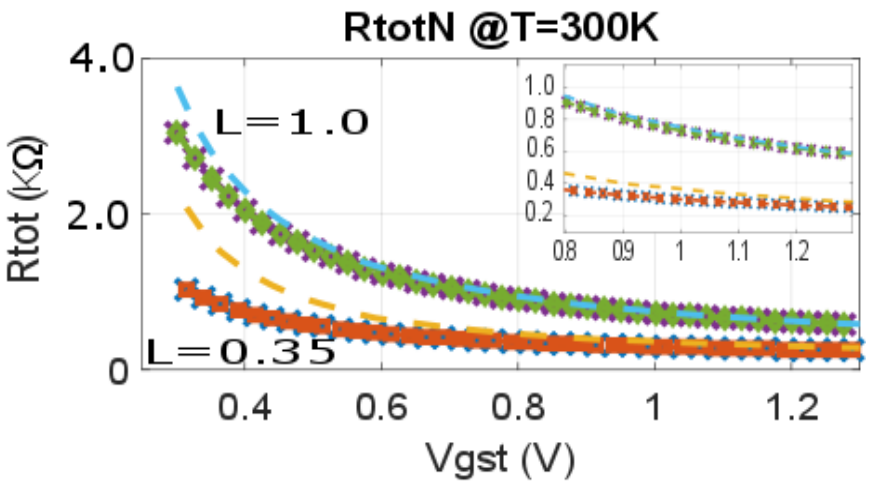
$$R_{ch0} = \frac{1 + (\theta V_{gst})^{n-1}}{\mu_g C_{ox} W \theta^{n-2} V_{gst}^{n-1}}$$

Total channel Resistance



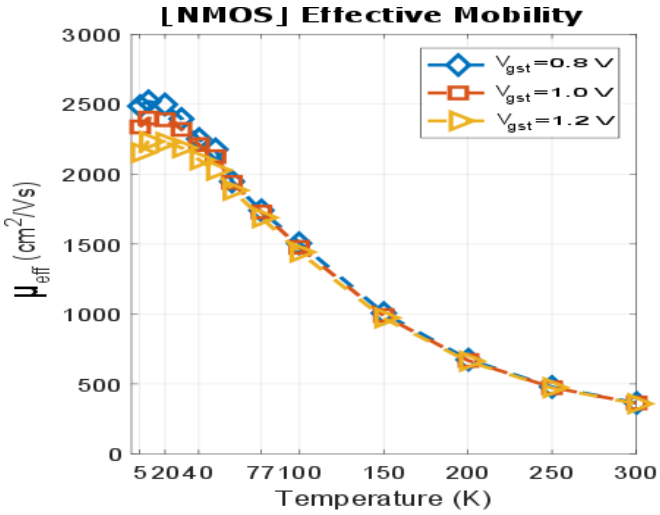






CMOS parameter extractions & Modelling

Mobility



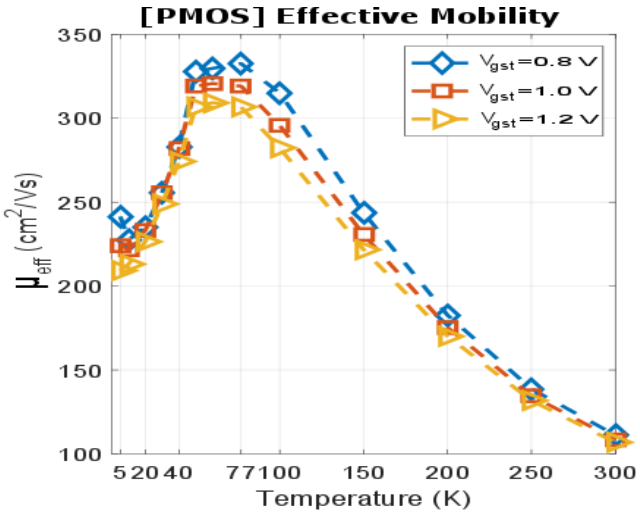
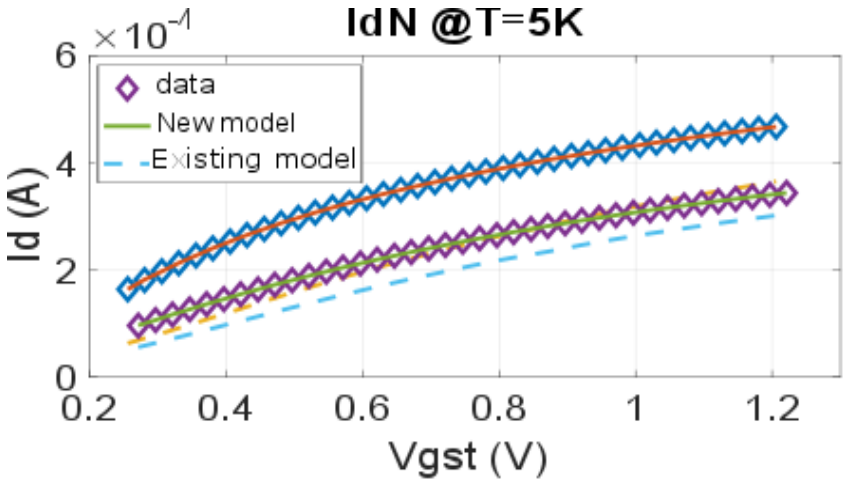
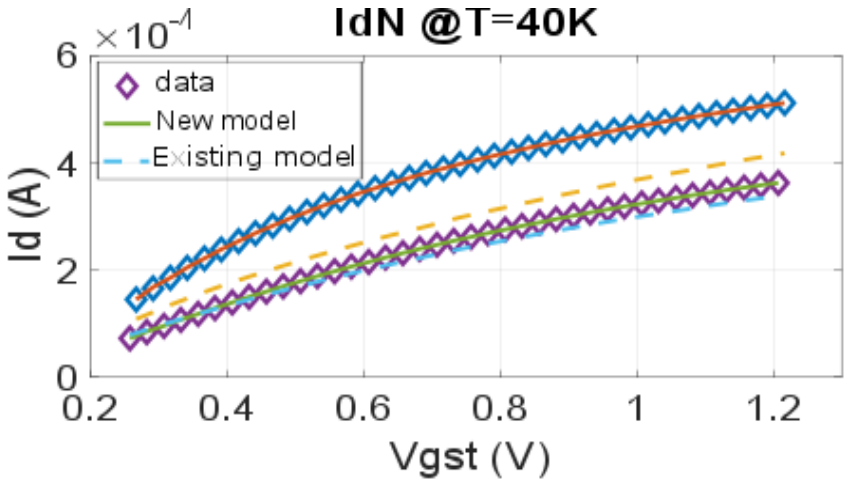


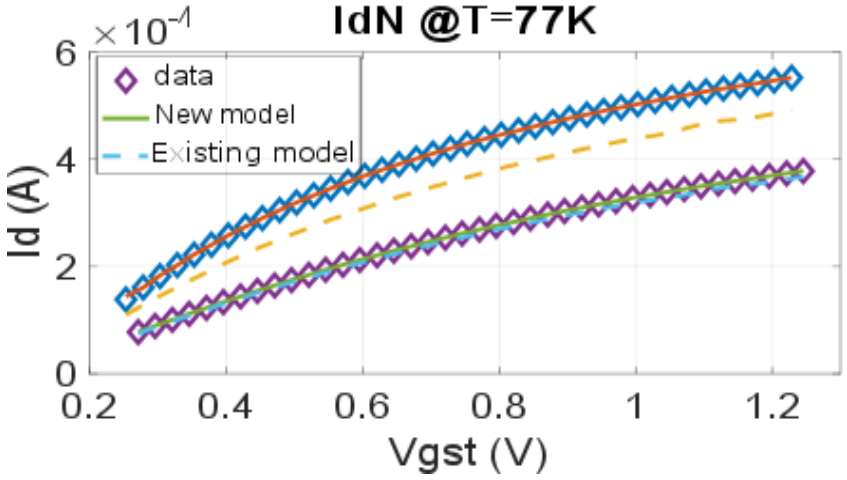
TABLE I. MOSFET PARAMETERS

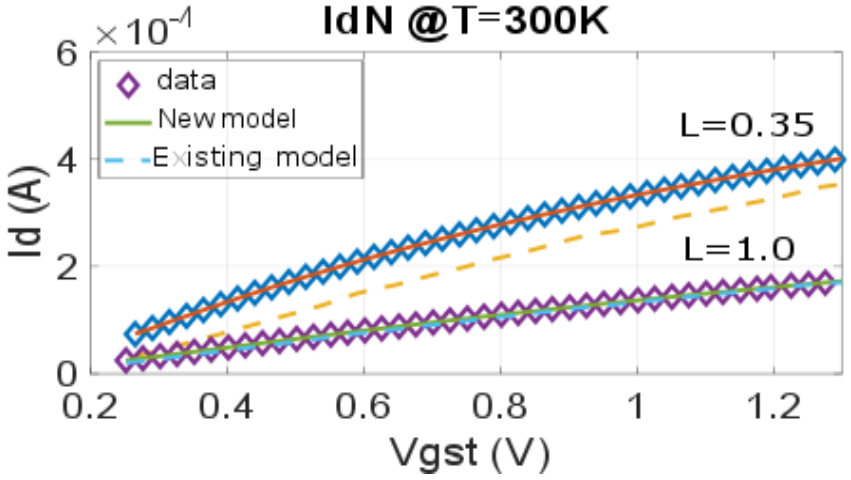
T (K)	5	40	60	77	100	200	300
n	3	3	2.75	2.5	2.1	2	2
NMOS							
θ (V^{-1})	1.48	1.2	0.96	0.72	0.28	0.06	0.04
μ_g (cm^2/Vs)	5068	4502	3868	3291	2089	708	376
PMOS							
θ (V^{-1})	1.58	1.13	1.11	0.99	0.63	0.25	0.13
μ_g (cm^2/Vs)	498	568	653	638	499	220	123

Id-Vg model


IdN @T=5K
×10^-4
data
New model
Existing model
Id (A)
Vgst (V)

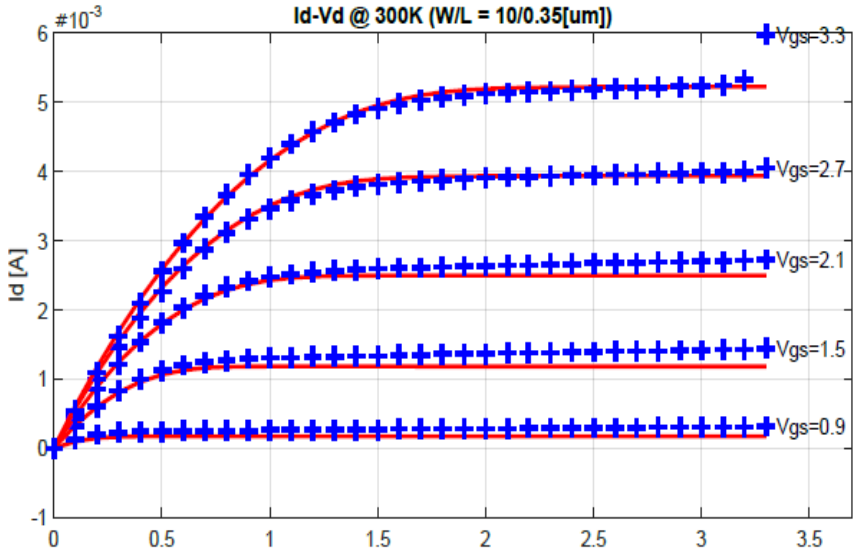

IdN @T=40K
×10^-4
data
New model
Existing model
Id (A)
Vgst (V)

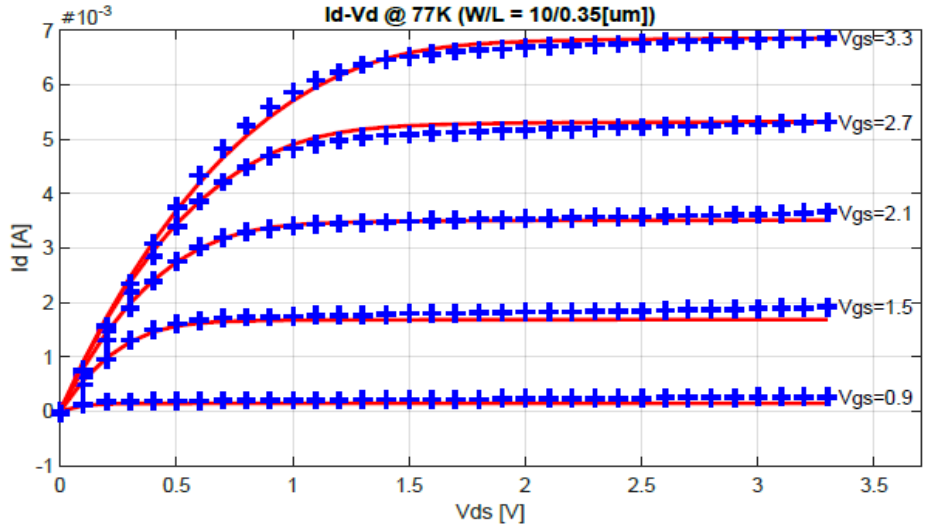

IdN @T=77K
×10^-4
data
New model
Existing model
Id (A)
Vgst (V)

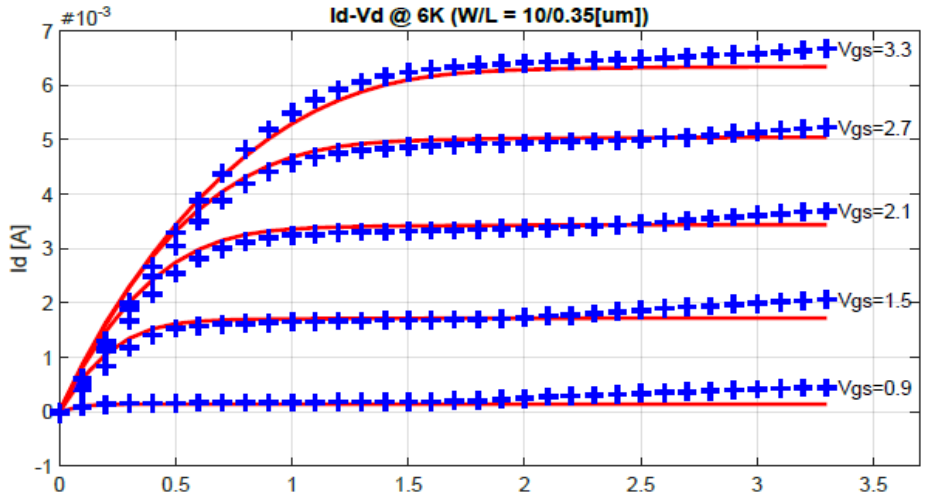

IdN @T=300K
×10^-4
data
New model
Existing model
L=0.35
L=1.0
Id (A)
Vgst (V)

Id-Vd Model:

A simple SPICE model (VerilogA) is developed and incorporated into Cadence Spectre simulator







Error in Current Matching Model

Current matching model:

$$\sigma^2_{\left(\frac{\Delta I_d}{I_d}\right)} = (1 - G_d R_{sd})^2 \sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_d}\right)^2 \sigma^2_{V_{tl}} + G_d^2 \sigma^2_{\Delta R_{sd}} + 2G_d^2 \rho_{(\Delta R_{ch}, \Delta R_{sd})} \sigma_{\Delta R_{ch}} \sigma_{\Delta R_{sd}}$$

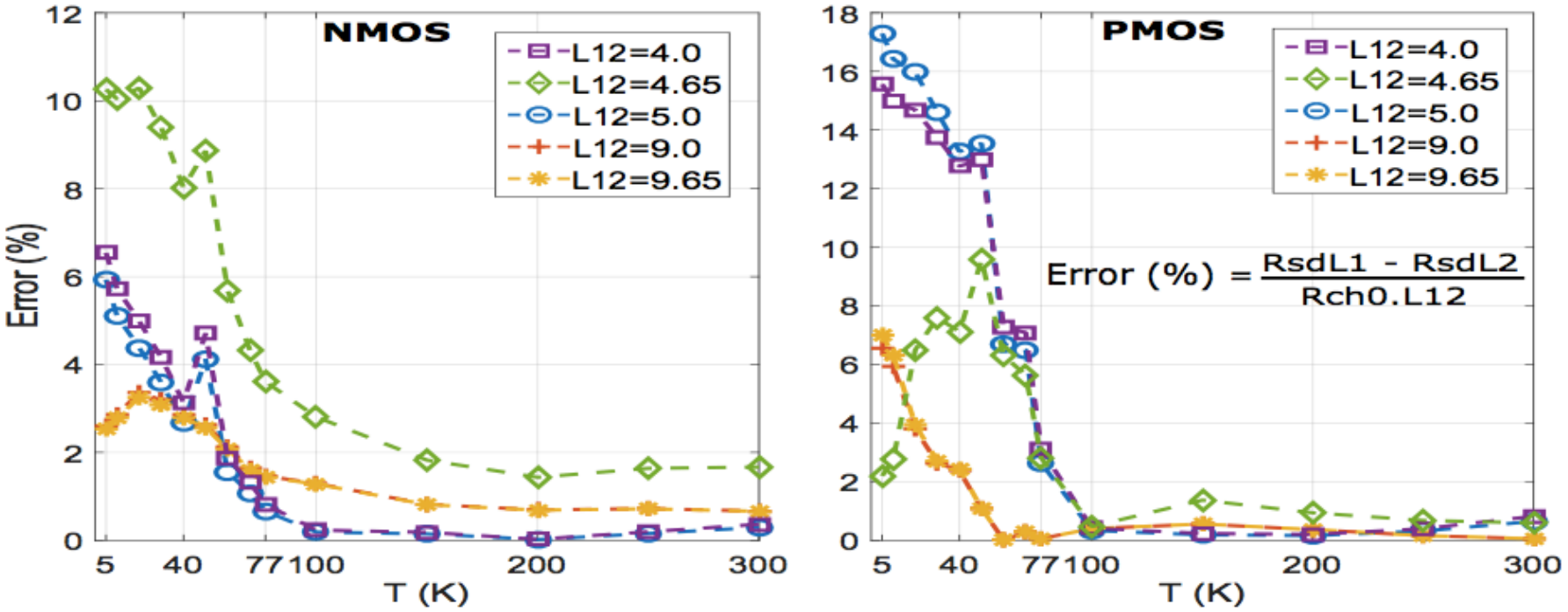
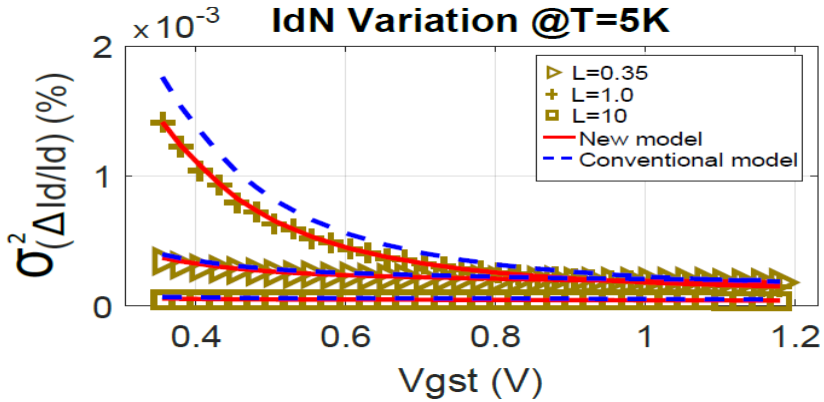
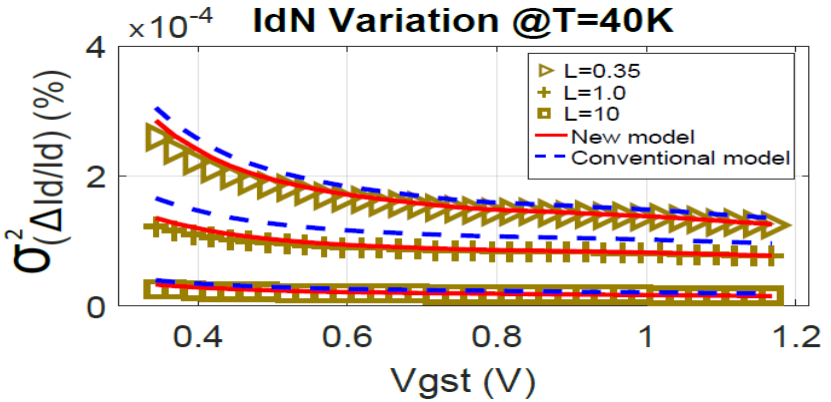


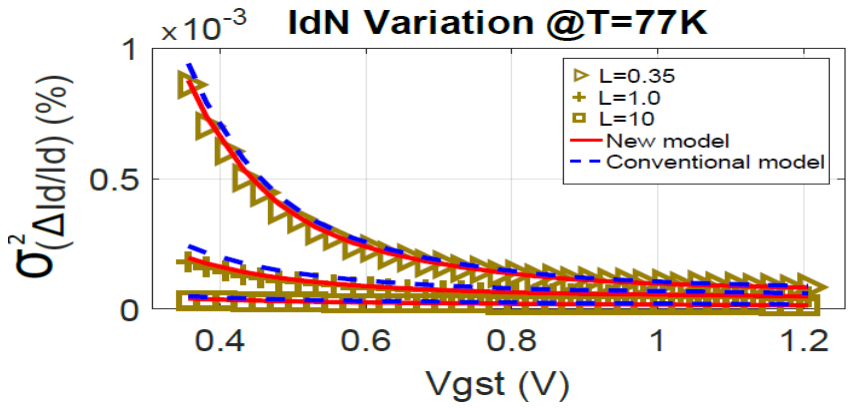
Fig. 2. Error in R_{ch0} approximation at $V_{gst} = 1$V.

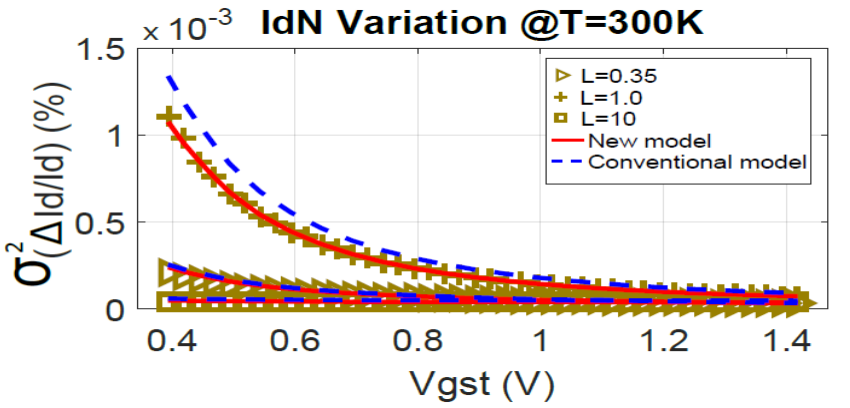
Current matching model:

$$\sigma^2_{\left(\frac{\Delta I_d}{I_d}\right)} = (1 - G_d R_{sd})^2 \sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_d}\right)^2 \sigma^2_{V_{tl}} + G_d^2 \sigma^2_{\Delta R_{sd}} + 2G_d^2 \rho_{(\Delta R_{ch}, \Delta R_{sd})} \sigma_{\Delta R_{ch}} \sigma_{\Delta R_{sd}}$$









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Summary

- Have developed and verified
  - first wide-temperature range bulk CMOS transistor model
  - first bulk CMOS transistor current matching model

THE UNIVERSITY OF SYDNEY

References

[1] Hornibrook, J. M., et al. "Cryogenic Control Architecture for Large-Scale Quantum Computing." *Physical Review Applied* 3.2 (2015): 024010.

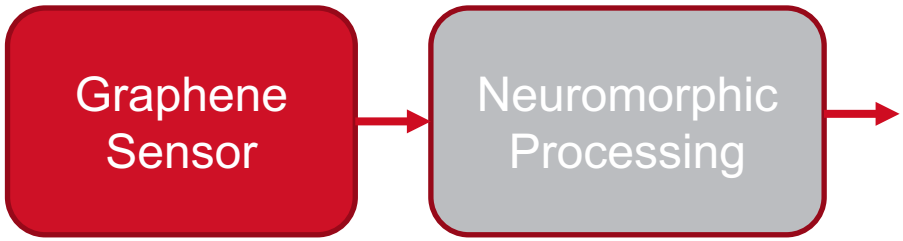
[2] Dao, Nguyen Cong, et al. "An enhanced MOSFET threshold voltage model for the 6–300K temperature range." *Microelectronics Reliability* , vol. 69, pp. 36-39.

[3] Nguyen Cong Dao, Abdallah El Kass, Craig T. Jin and Philip H.W. Leong, “Impact of Series Resistance on Bulk CMOS Current Matching over The 5–300 K Temperature Range,” submitted to IEEE Electron Device Letters.

Sensors

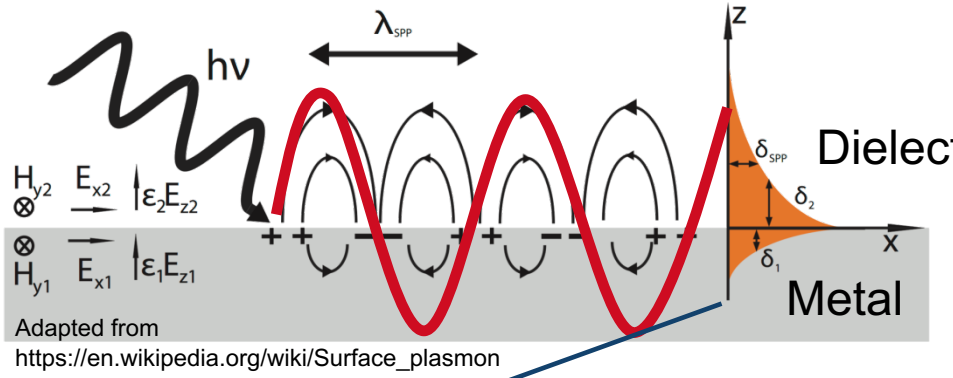
Motivation

› Sensor with in-built processing



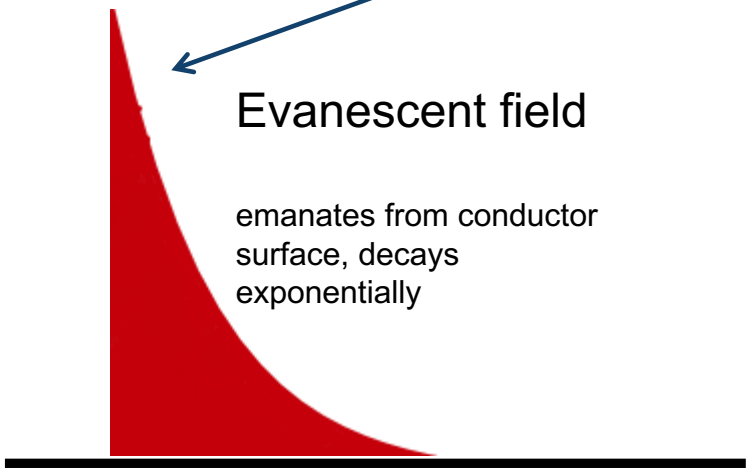
Surface Plasmon Resonance

Surface Plasmon Polariton



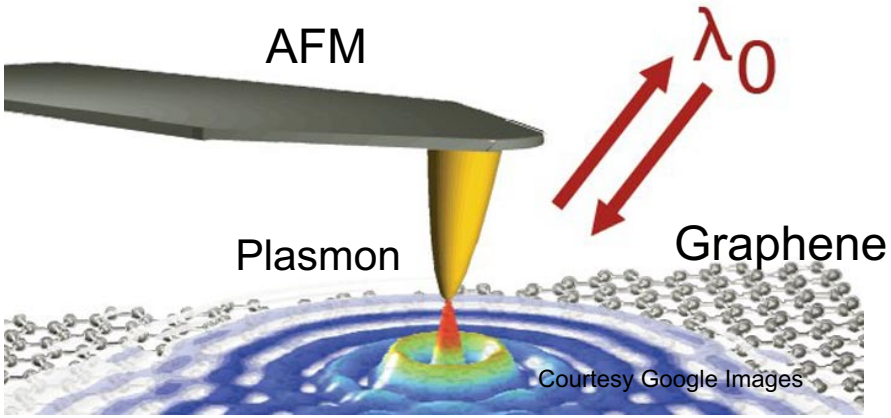
Adapted from
https://en.wikipedia.org/wiki/Surface_plasmon

Conductors - largely fixed nuclei in a sea of free electrons. Electron gas is a plasma and wave-like coherent oscillations called plasmons can be formed by adding energy (particularly strong at surface). When the frequency of the energy source matches the resonant frequency of the surface plasmons, energy transfer is maximized.



Evanescent field

emanates from conductor surface, decays exponentially

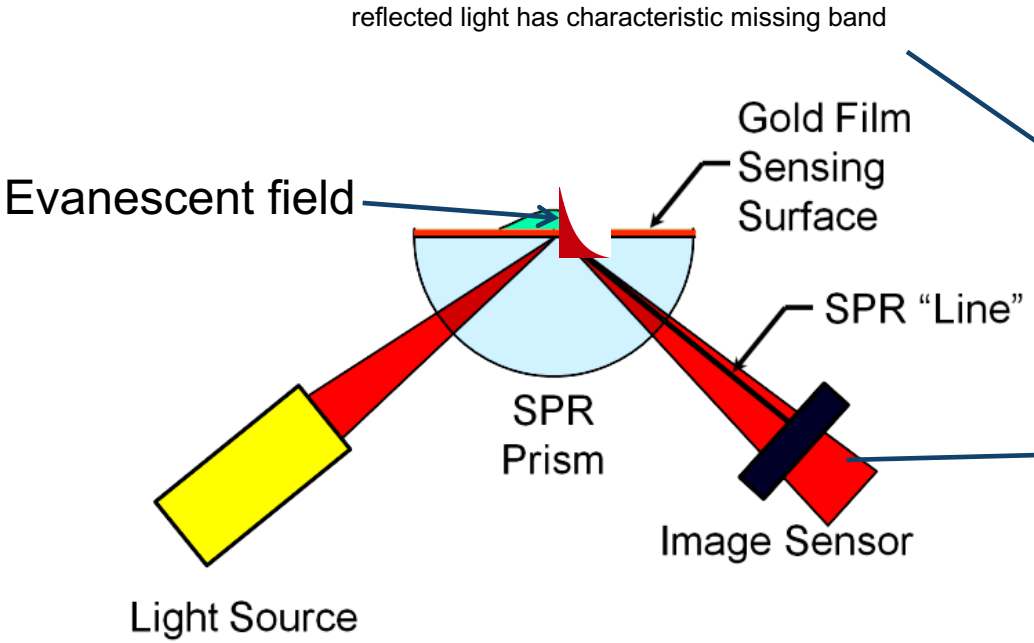


Courtesy Google Images

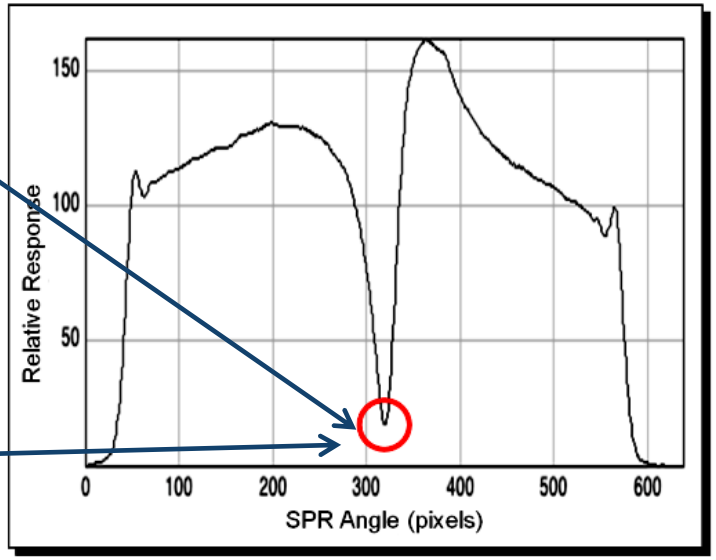
Surface Plasmon Resonance as a Sensor

Kretschmann biosensor

Incident light from below excites SPP
reflected light has characteristic missing band



The Surface Plasmon Resonance Technique

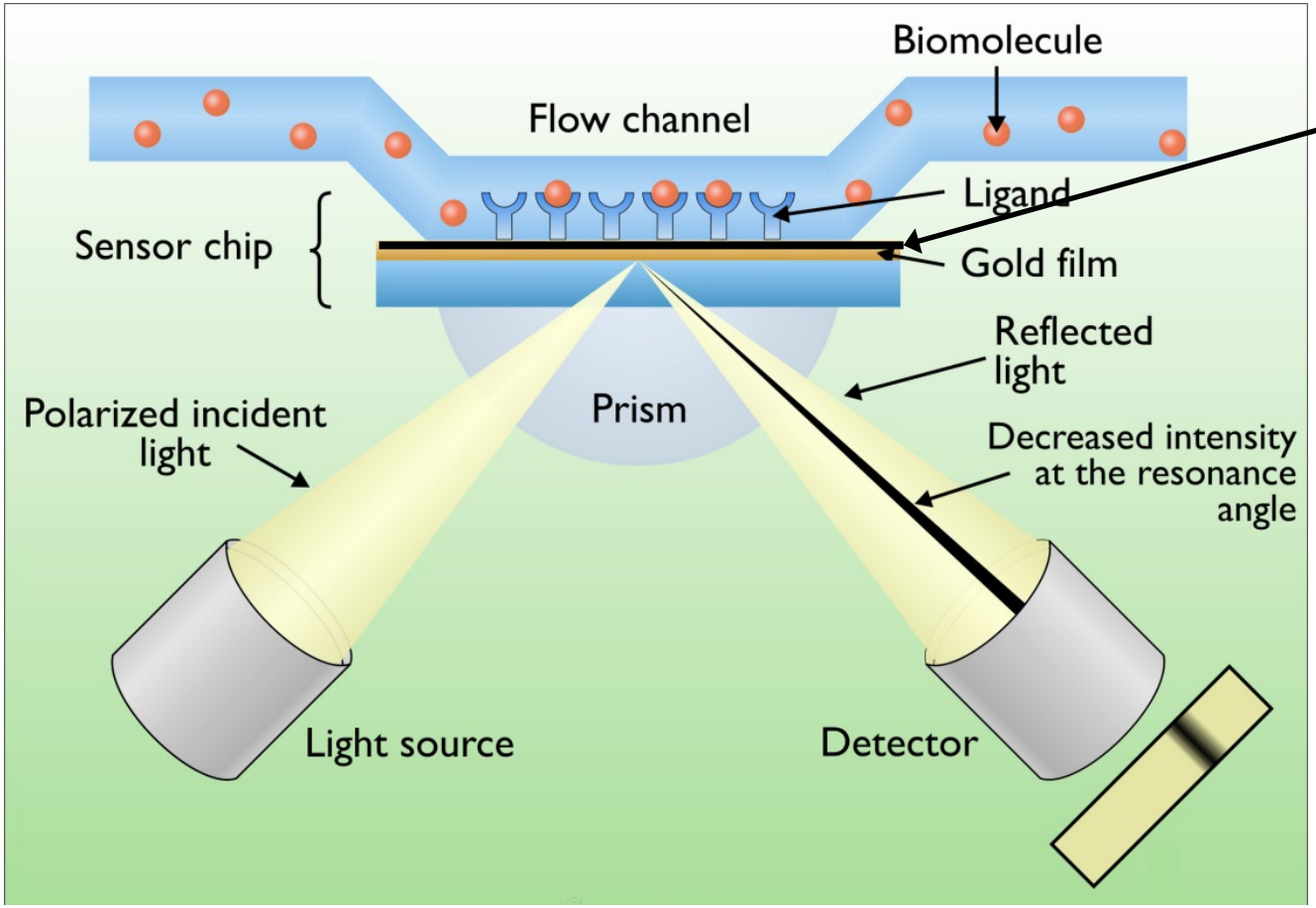


Typical SPR Image

When SPR occurs at the conductor, a dark band will be detected, indicating the SPR frequency.

Courtesy Google Images

Surface Plasmon Resonance Biosensor



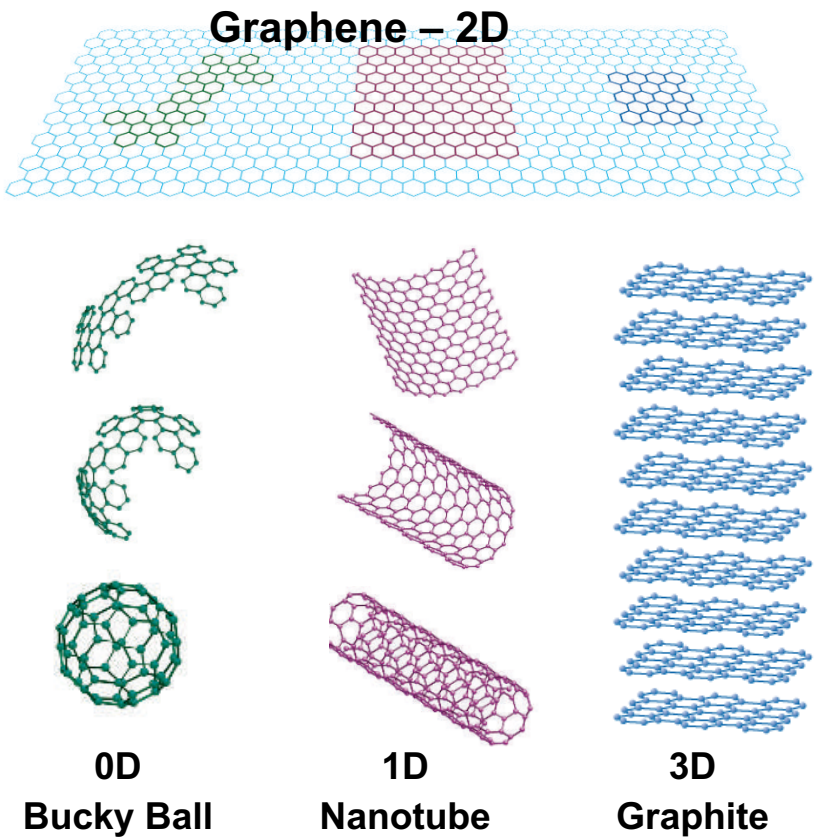
Graphene layer

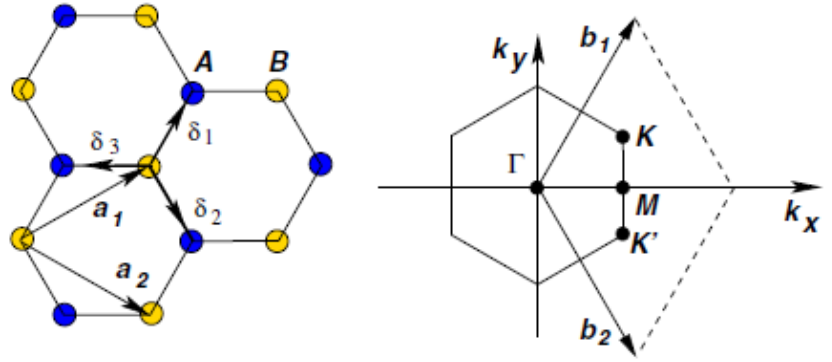
Courtesy Google Images

Nanoscale changes (such as the binding of different molecules to the surface) alters the SPR frequency

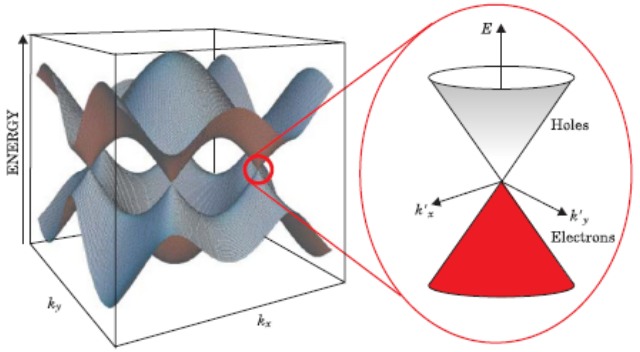
Graphene

The first 2D material (no bandgap but doping can introduce one)





Unit cell, sublattice structure and Brillouin zone



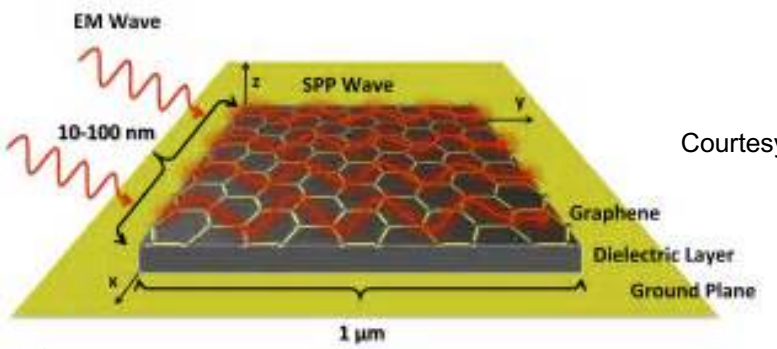
Band structure

Dirac cones near K and K'

Geim & Novoselov, Nature Materials, 2007. **6**(3)

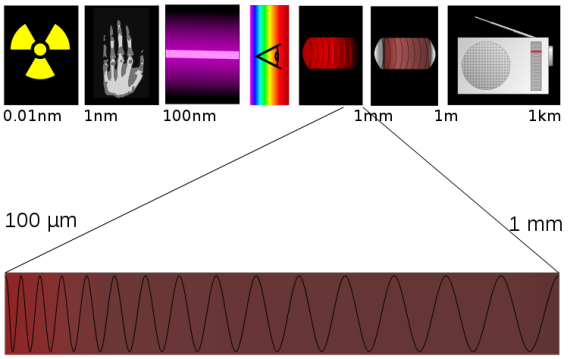
Das Sarma *et al.* Reviews of Modern Physics, 2011. **83**(2)

Graphene SPR



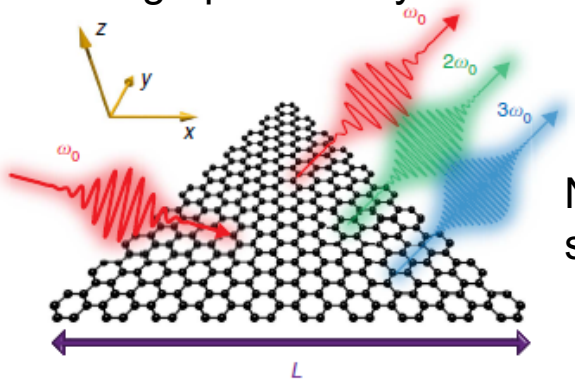
SPP in micron scale graphene, resonant frequency far IR or THz band.

Courtesy of Google Images



The THz band, far IR to near microwave

Nanoscale graphene may enable a shift in frequency

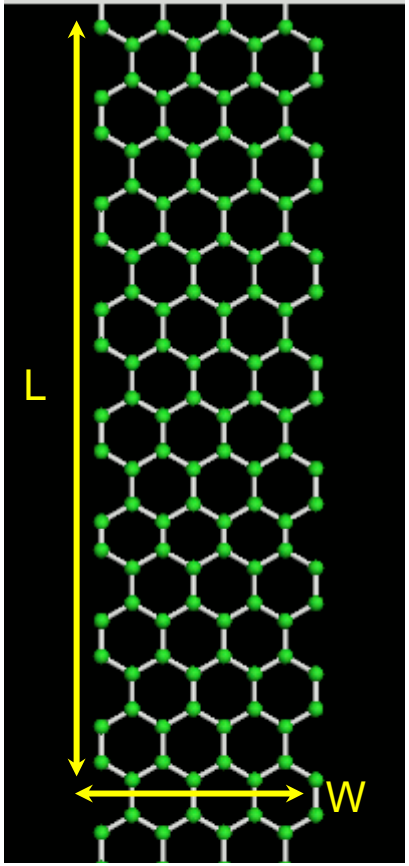


Non-linear optic effect, 4-wave mixing shown in nanoscale graphene

Cox & de Abajo Nature Communications, 2014. **5**(5725).

Unlike metal nanostructures, graphene can be highly conductive, generates long-lasting plasmons and appears to be able to produce a tunable SPR after fabrication.

Graphene Nanoribbons



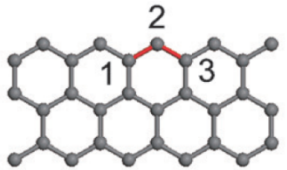
Graphene nanoribbon (GNR)

- Width: < 10 nm
- Aspect ratio: L/W (40 -> 1,000)
- Defects
- Doping
  - Chemical
  - Electrostatic

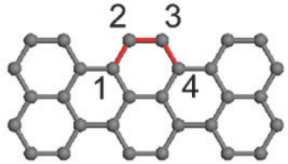
Single-layer graphene nanoribbons have small width (1D structure), changes electronic properties.

Edges

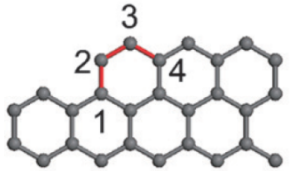
Zigzag



Armchair



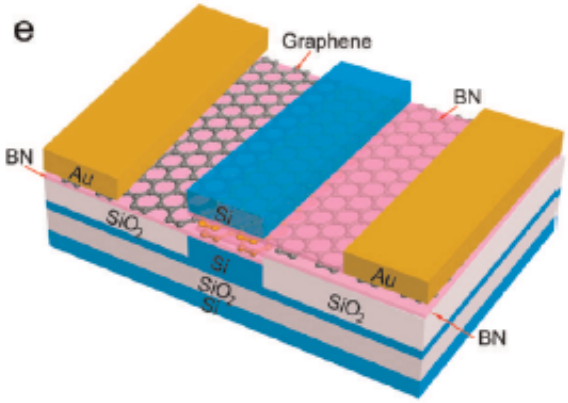
Random



Qiu *et al.* Angewandte Chemie-International Edition, 2016. **55**(34)

Graphene Nanoribbons

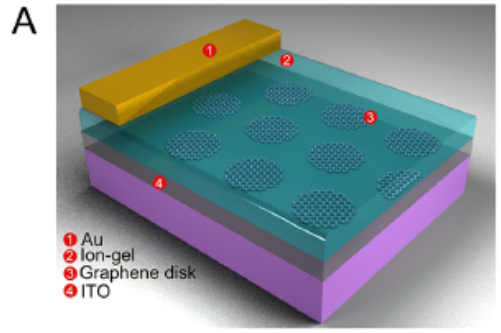
GNR-based transistor-like devices

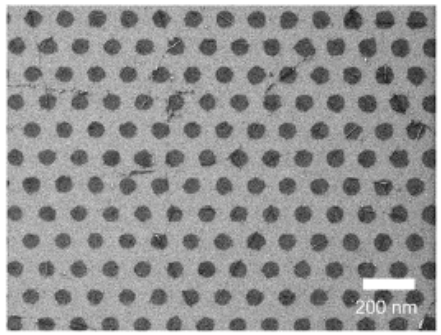


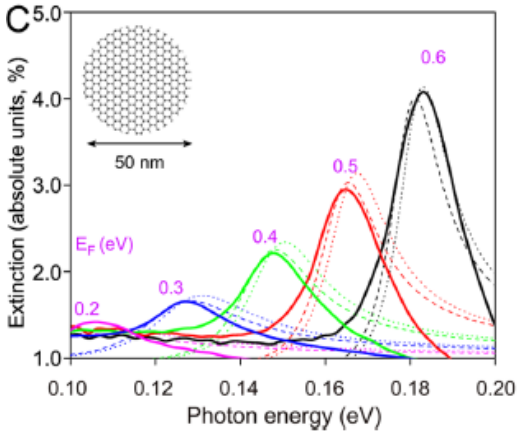
Silicon-gated, BN complemented

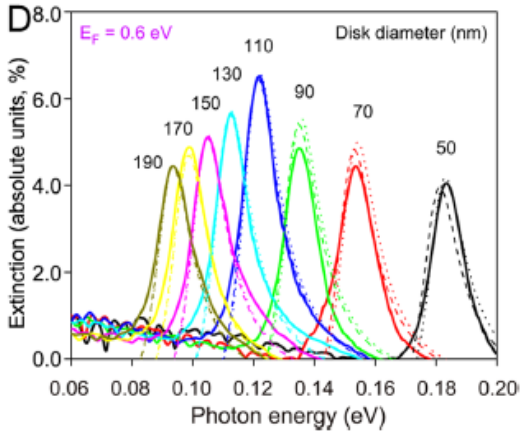
Bao & Loh ACS nano, 2012. **6**(5)

Transistor-like devices - gate voltage changes Fermi energy levels (affecting electronic and photonic properties).









Gel-gated nanodisks

0.2 eV ≈ 6 μm λ - far IR

Fang *et al.* ACS nano, 2013. **7**(3)

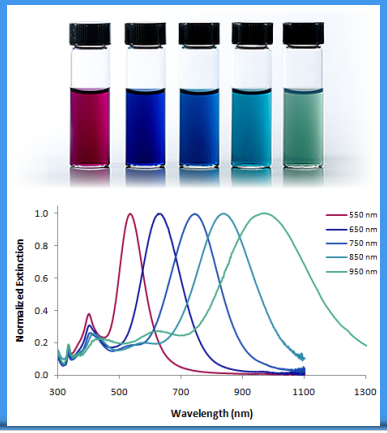
The Project

Current state of the art in SPR:

Metal nanostructure

Advantage:
- λ_R in visible or near IR

Disadvantages:
- High ohmic losses
- Short plasmon lifetime
- Not tunable post fabrication

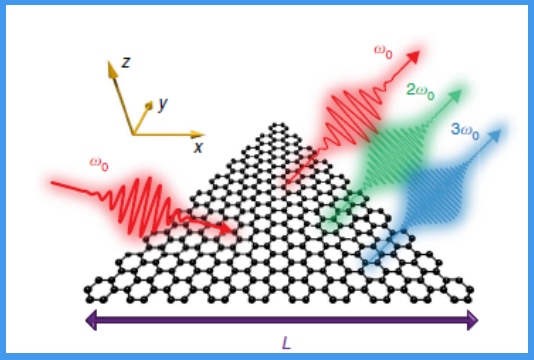


Possible development in SPR:

Graphene nanoribbon

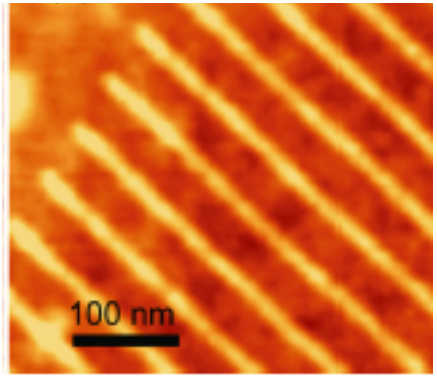
Advantage:
- Highly conductive
- Long lasting plasmon
- Electronically tunable

Disadvantage:
- λ_R in far IR/THz



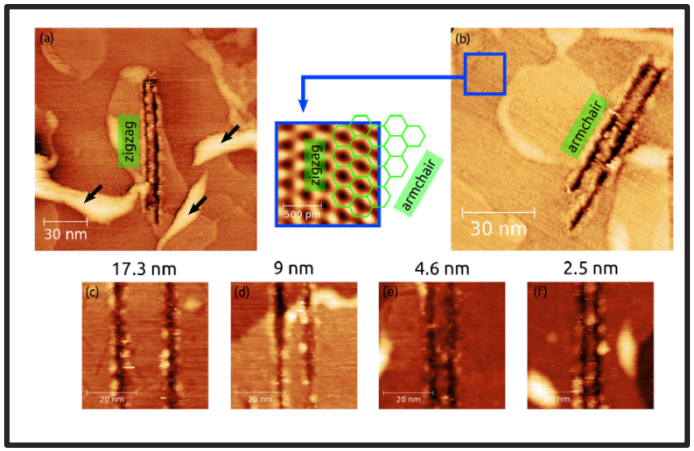
The Project Goals

1. Fabricate GNRs (< 5nm)



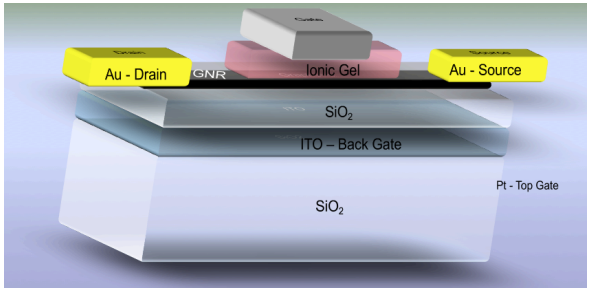
Archanjo *et al.* Applied Physics Letters, 2014. **104**(19)

2. Determine GNR morphology (theory only for armchair edging)



Nemes-Incz *et al.* Applied Surface Science, 2014. **291.**

3. Incorporate GNRs into Active SPR Device



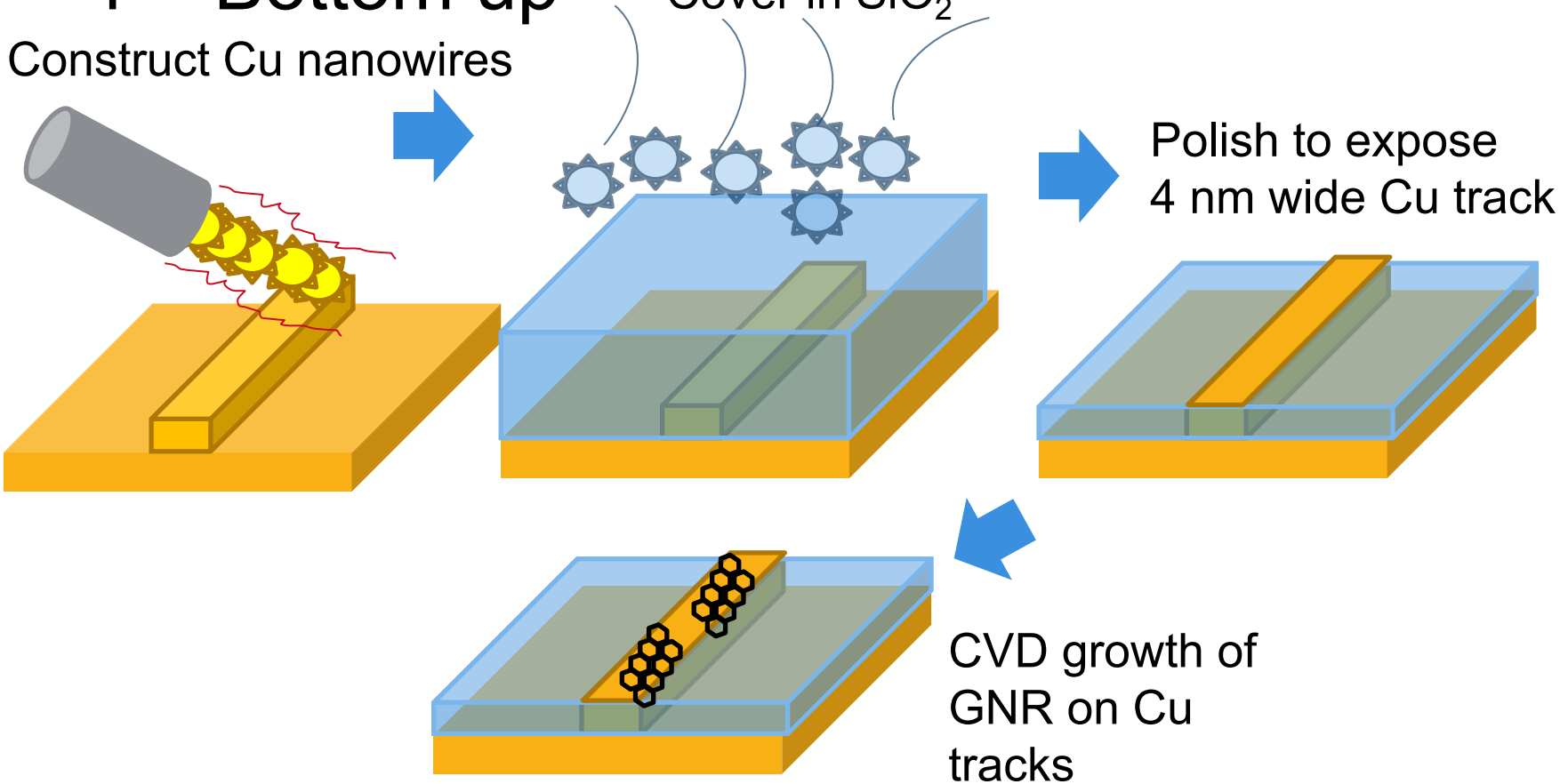
4. Determine device characteristics – test against model. Have we achieved a new and worthwhile technology?

$$\lambda_R = 350\sqrt{W \cdot \frac{(1+\varepsilon_S)}{E_F}}$$

Fabrication possibilities

1 – Bottom up

Construct Cu nanowires



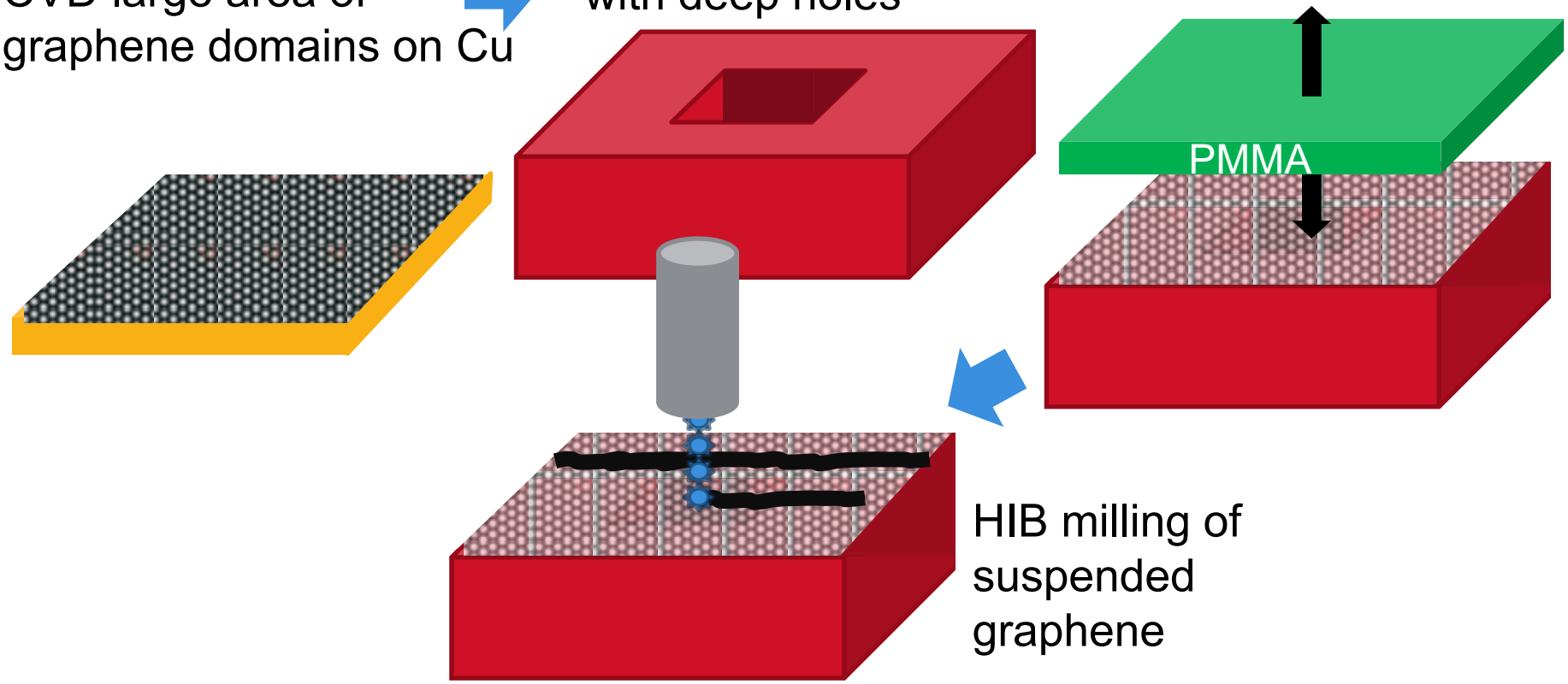
Fabrication possibilities

2 – HIB Lithography

CVD large area of graphene domains on Cu

Construct substrate with deep holes

Transfer graphene sheet



HIB milling of suspended graphene

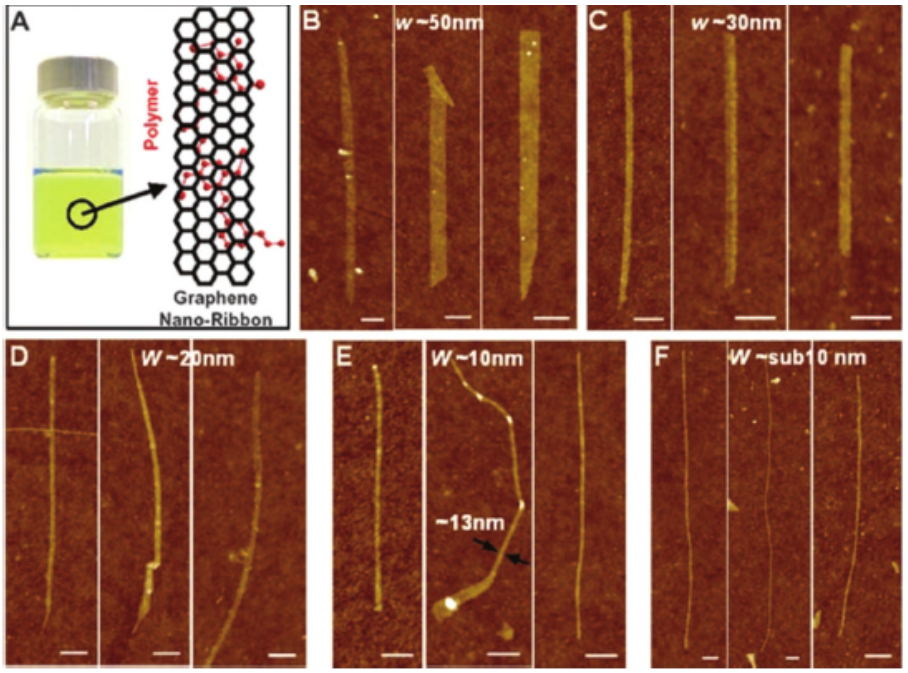
Fabrication possibilities

3 – In Solution

Chemical exfoliation of graphite

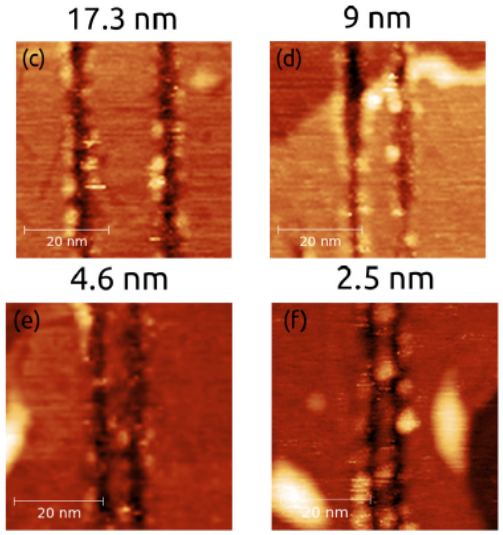
Sonication in solution

Extraction from solution and size sorting



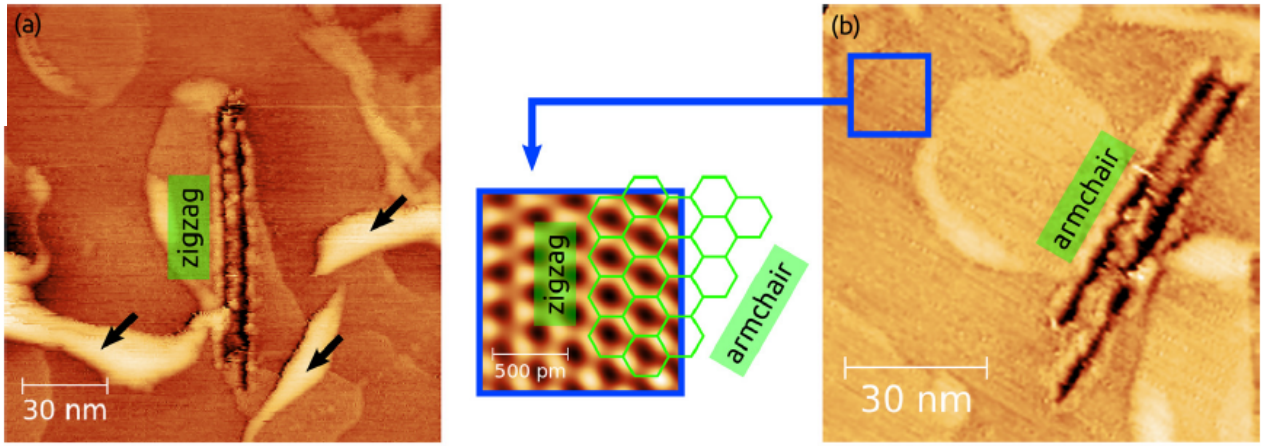
Yagmurcukardes *et al.* Applied Physics Reviews, 2016. **3**(4)

GNR morphology – STM and TERS



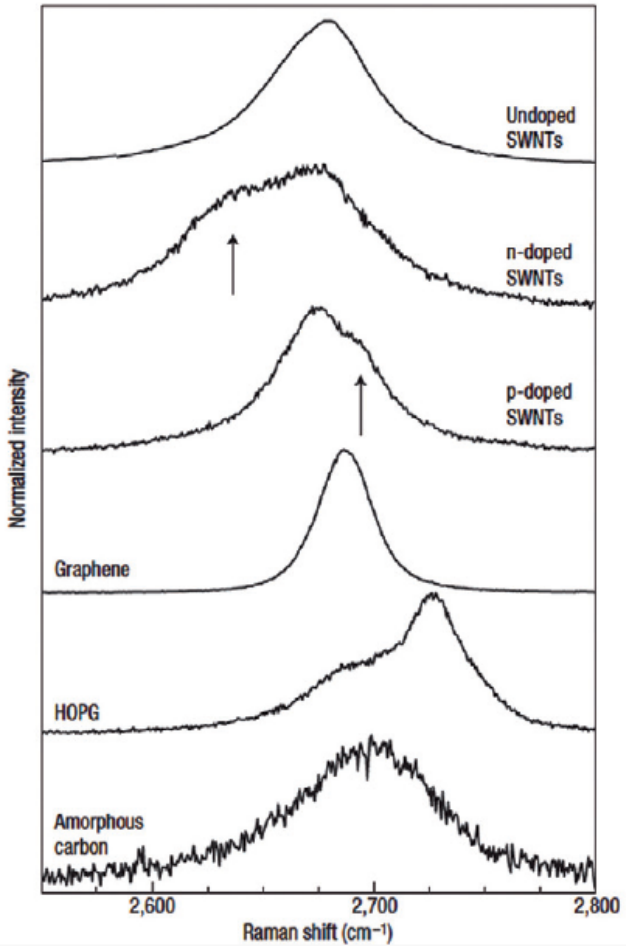
Ribbon widths.
Looking for < 5 nm, smooth clean edges

Nemes-Incz *et al.* Applied Surface Science, 2014. **291.**



Edge morphology. Observe consistency (or random) and type.

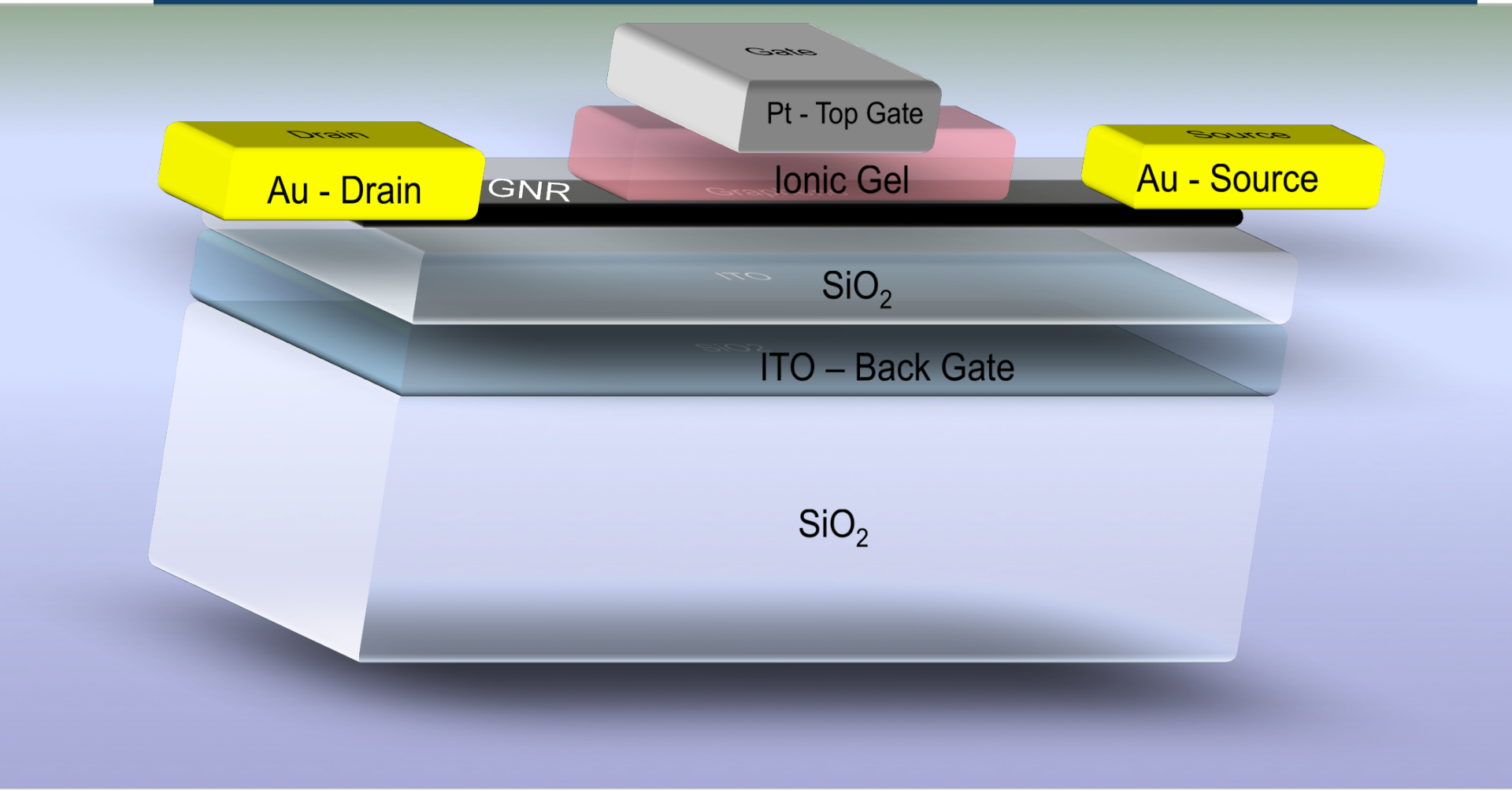
GNR morphology – STM and TERS



Physical and chemical defect status. Oxidation? Multidomain? Gaps?

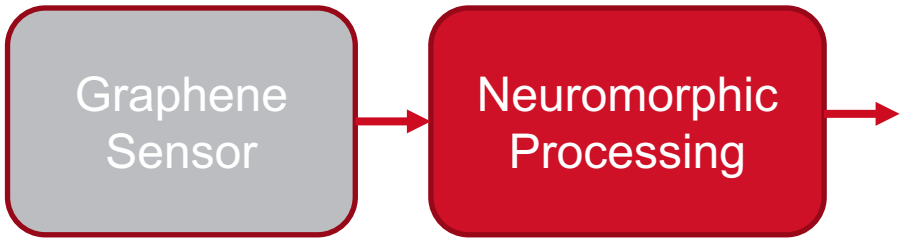
Araujo *et al.* Materials Today, 2012. **15**(3)

Active gated SPR device



Motivation

› Sensor with in-built processing

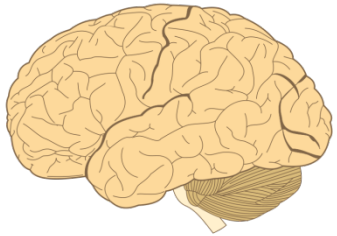


Memristor as Synapse in Spiking Neural Networks

Human Brain:

10^{14} Synapses and 10^{10} Neurons

- 20 Watts of power (10 Hz)!
- 15 centimetres long!
- Non-volatile learning memory!

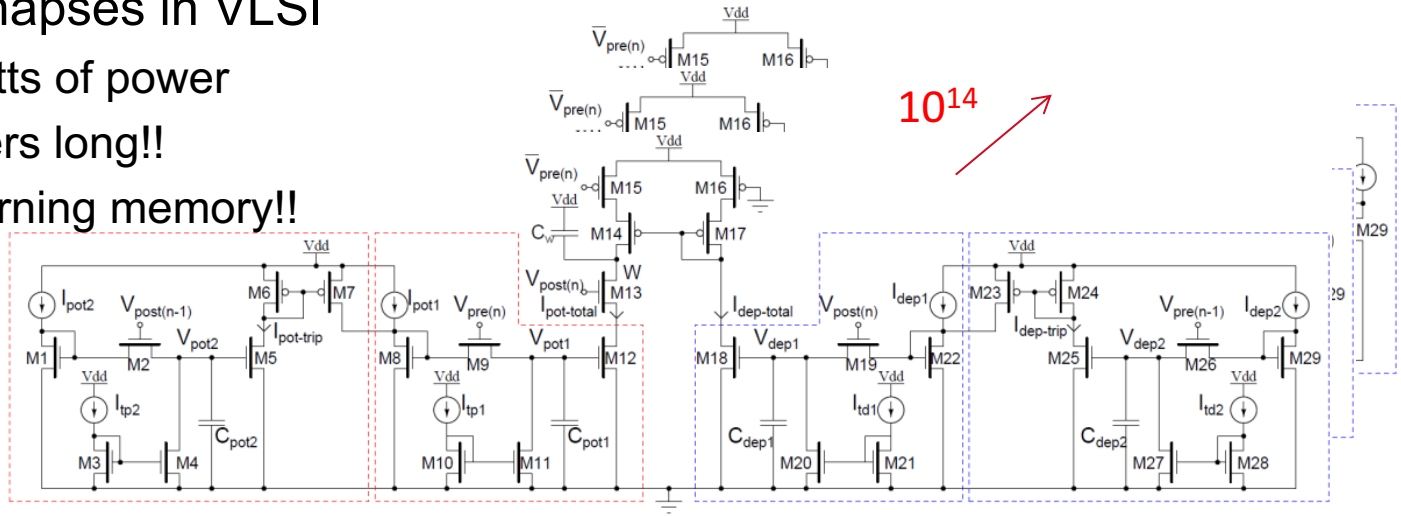


http://commons.wikimedia.org/wiki/File:Human-brain.SVG

An artificial Brain-scale SNN:

10^{14} Learning Synapses in VLSI

- 60 Kilo Watts of power
- 5 Kilo meters long!!
- Volatile learning memory!!

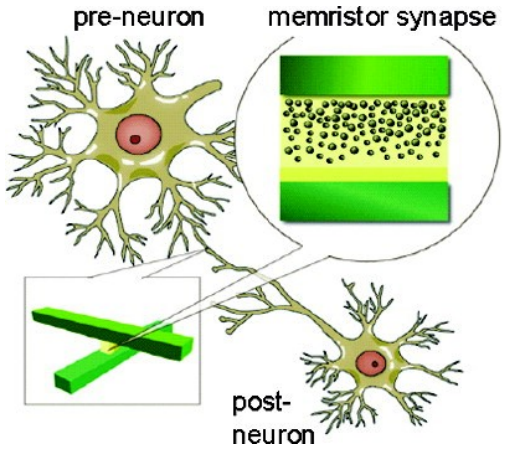


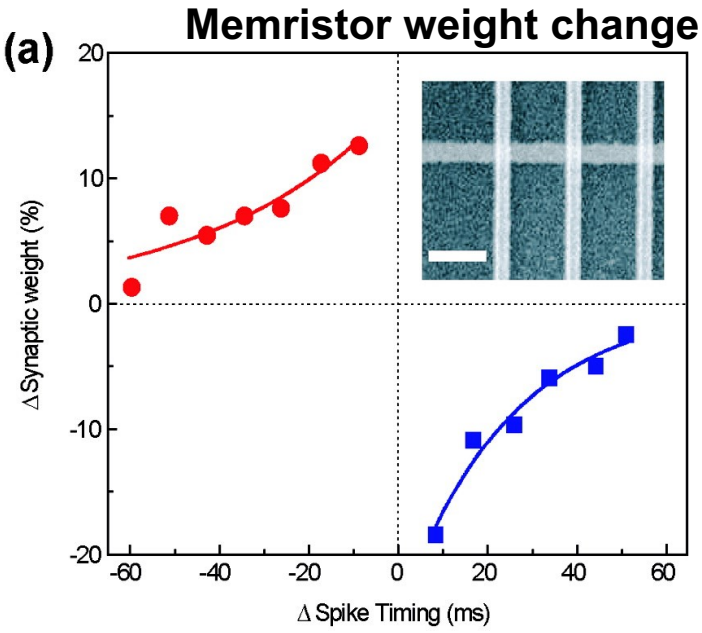
Memristor as Synapse in Spiking Neural Networks

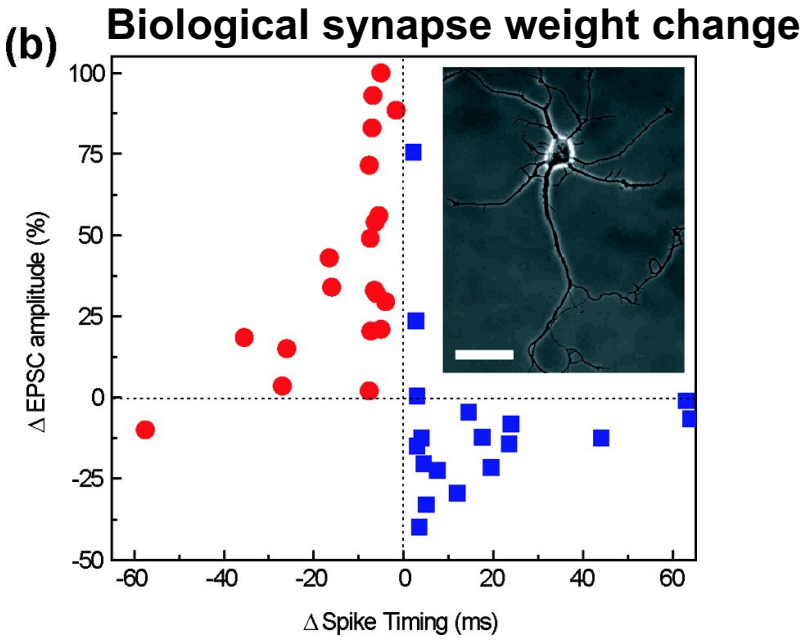
Memristive synapse:

10^{10} Memristive synapses

- Non-volatile memory!
- A few square centimetres of area
- Lower power consumption than VLSI
- Compatible with synaptic plasticity dynamics such as STDP



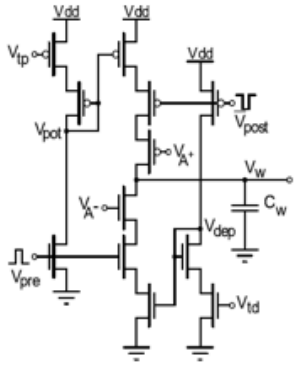


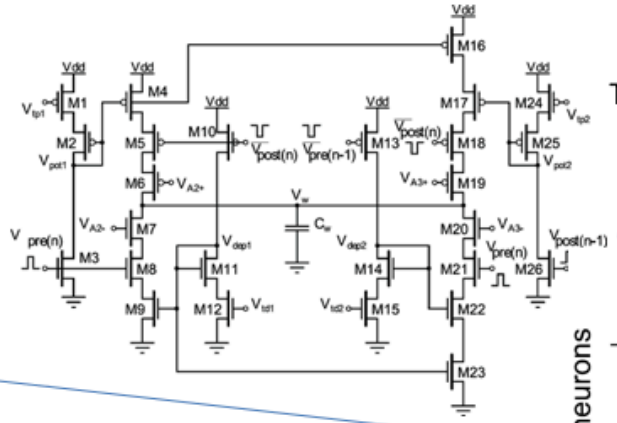


All three Images are extracted from Jo et al., Nano letters (2010)

Forming a SNN with Memristive Synapses

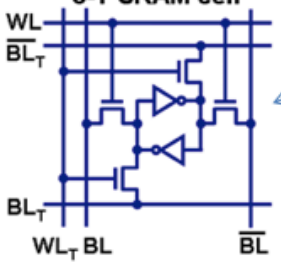
PSTDP circuit, Indiveri et al., IEEE TNN, 2006



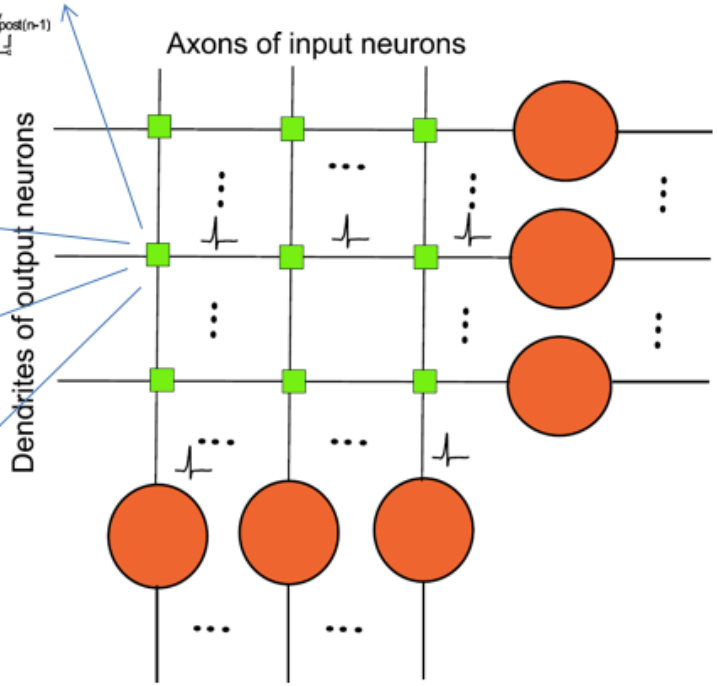


TSTDP circuit, Azghadi et al., IJCNN, 2012

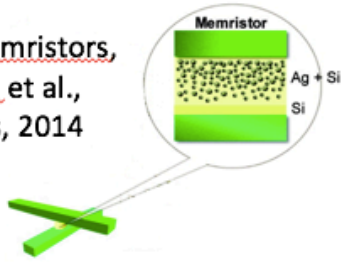
Transposable 8-T SRAM cell



Memory element for digital STDP
By IBM, Seo et al., IEEE CICC, 2011



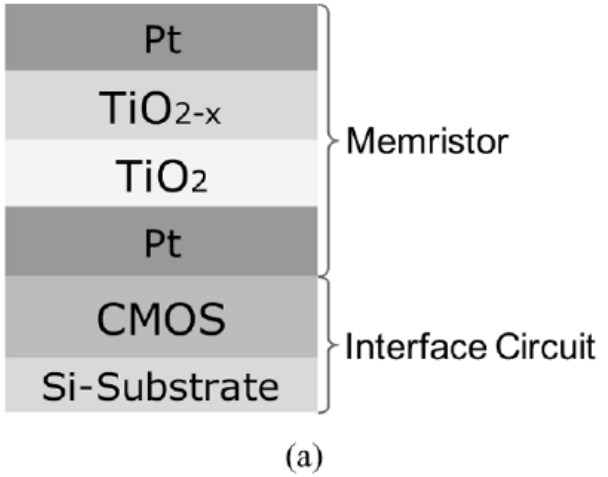
PSTDP using ideal memristors, Serrano-Gotarredona et al., Memristive Networks, 2014

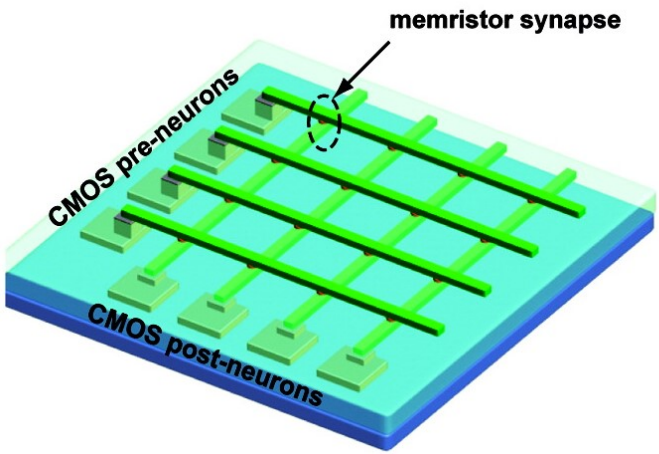


But, neurons are CMOS, synapses are memristor!
How to connect them?

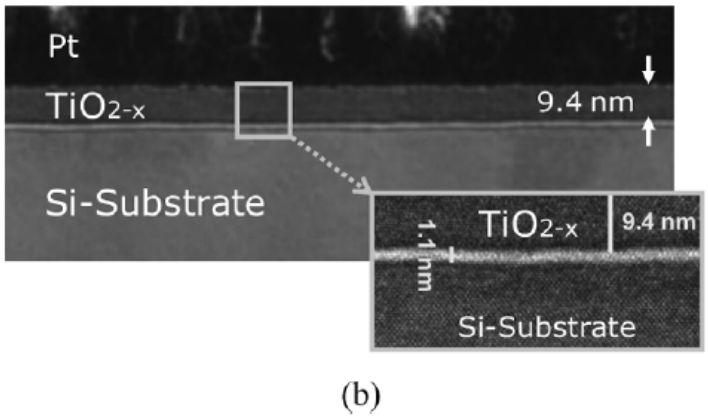
Forming a hybrid CMOS-memristor SNN

Hybrid CMOS-Neuron SNN:
Neurons: CMOS
Synapses: Memristors





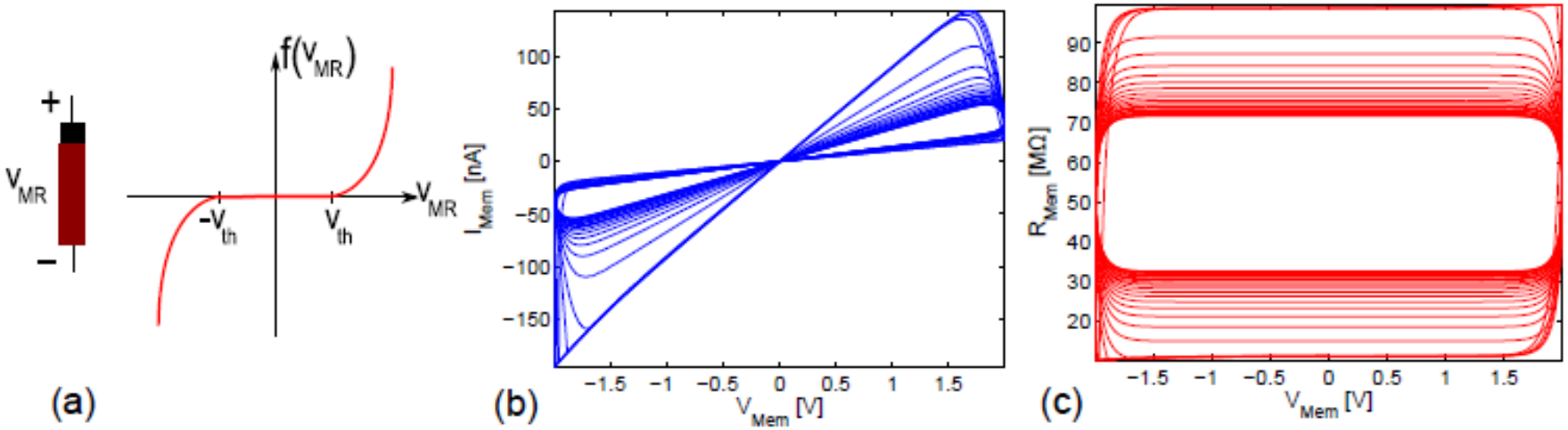
Memristor-Mos implementation by
Jo et al., Nano letters, 2010

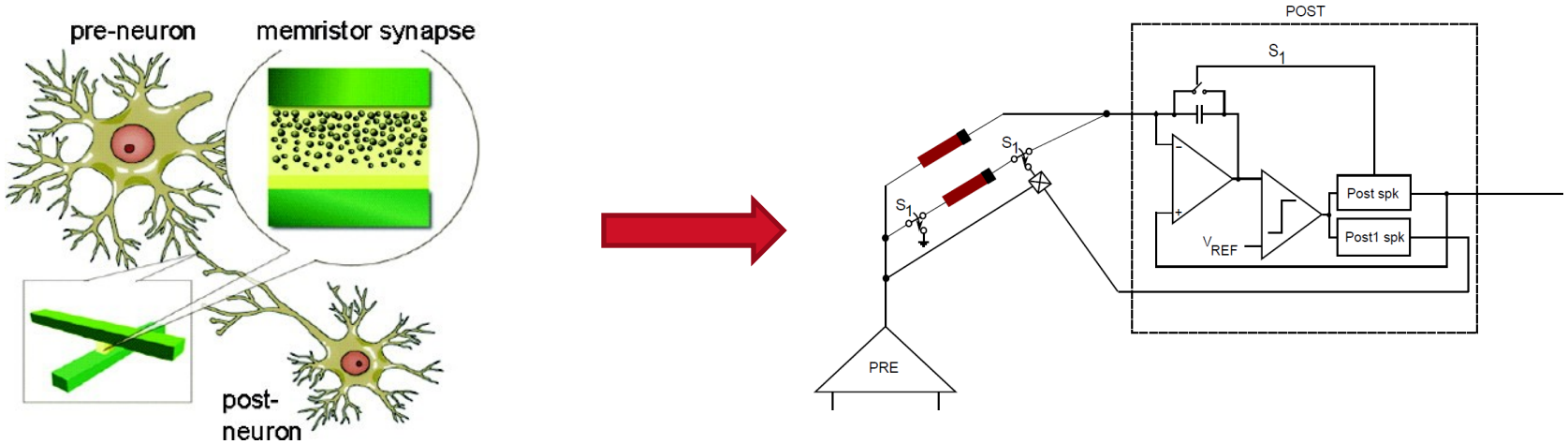


Memristor-Mos implementation by
Eshraghian et al., IEEE TVLSI, 2011

Forming a hybrid CMOS-memristor SNN

A typical memristor behaviour

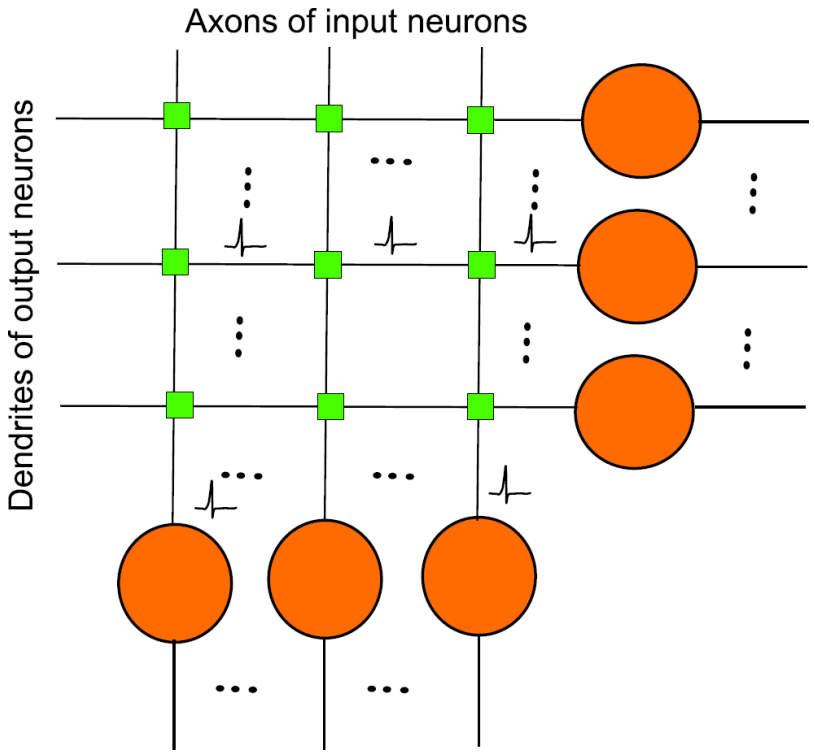


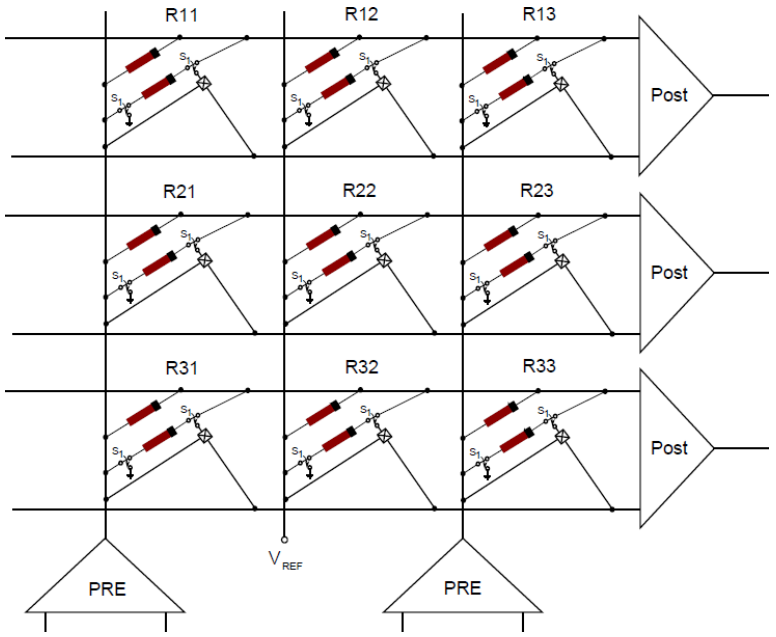


Our recent hybrid CMOS-Memristor Spiking Neural Network, IEEE Transactions on Biomedical Circuits and Systems, 2016

Forming a hybrid CMOS-memristor SNN

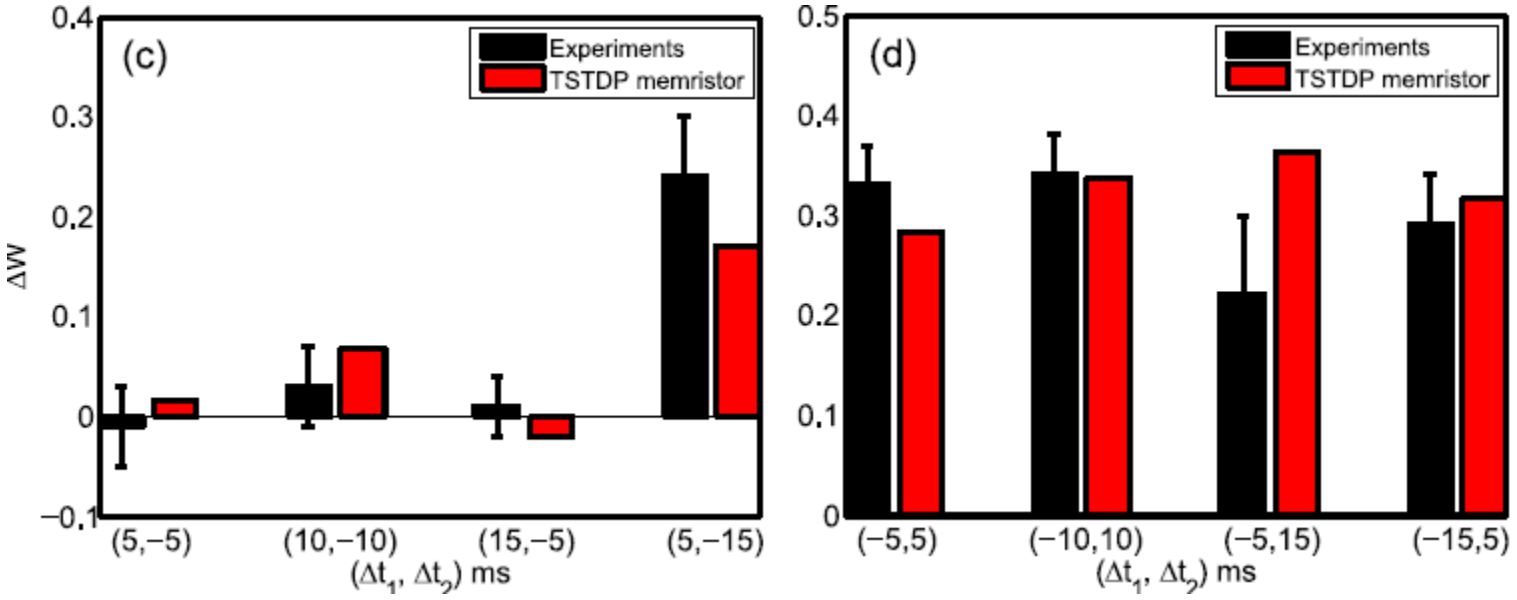
A network of CMOS neurons and memristive synapses





Our recent hybrid CMOS-Memristor Spiking Neural Network, IEEE Transactions on Biomedical Circuits and Systems, 2016

Replicating Biological Experiments



- Experimental data obtained from mice hippocampus.
- Our circuit mimics triplet spike timing dependent plasticity (TSTDP) and spike-rate dependent plasticity

Summary

- Developing sensors with integrated processing
  - Surface plasmon resonance in graphene - optimisation of width and edge morphology
  - Tunable, low power, sensitive and selective sensor which can measure thousands of metabolic analytes with a single reading
- Spiking neural network with memrestive synapses and graphene-based inputs
- In the future, integrate sensing and powerful processing on a chip

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Conclusion

Conclusion

- Project aims to develop capabilities in the integration of nanotechnology with electronic integrated circuits through three subprojects
  1. Photonics - electrical interface to photonic signal processing chip
  2. LowT - analog transistor array for characterizing low-temperature devices
  3. Sensor – graphene based sensor

- Made progress in all three areas look forward to future AINST collaborations to extend our work

Spare slides