Significant Papers from the First 25 Years of the FPL Conference

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***Abstract*—The list of significant papers from the first 25 years of the Field-Programmable Logic and Applications conference (FPL) is presented in this paper. These 27 papers represent those which have most strongly influenced theory and practice in the field.**

I. Introduction

The first International Conference on Field-Programmable Logic and Applications (FPL) was held in 1991 at Oxford University. In the ensuing years, it has grown to be the largest meeting on field-programmable gate array (FPGA) technologies and systems, and many important contributions have been published at the conference.

This paper provides the list of the most significant contributions from 1991–2014. The selection was made by an international Significant Papers Committee (SPC), comprising the authors of this paper.

Only regular papers were considered and Google Scholar was used for citation counts. Since an objective process was desired, those papers having more than 9 citations per year, or more than 100 overall citations were included on an initial shortlist. Concurrently an open call to the community was made through the FPGA mailing list (fpga-list@mailman.sydney.edu.au), inviting nomination of papers with impact other than the number of citations. A total of 24 nominations were received and all papers that were not already on the initial shortlist (13 papers) were included in the final shortlist.

The resulting 60 shortlisted papers were divided into 5 categories, each with a corresponding subcommittee. SPC members served on a subcommittee according to their expertise. Since some nominated papers were authored by SPC members, subcommittee Chairs were chosen to have no conflict of interest with any of the papers within, and tasked with ensuring that no SPC member had conflicts of interest during the paper selection process. Following discussions within each subcommittee, recommendations were consolidated for the SPC. A final dialogue regarding the choices was then undertaken.

The total number of papers considered was 1,765 (this figure may be larger than the total number of full papers as it was not possible to distinguish them from posters in some cases). Through the process described, 27 papers were selected, this representing 1.5% of the total. Inevitably, the inclusion and exclusion of certain papers will be the subject of debate; however, this list represents the best efforts of the SPC to ensure a fair and objective selection process.

To meet publication deadlines, only the list of selected papers is presented here. A version with endorsements which will describe the impact of these papers on research and industrial development of FPL technologies and systems, is forthcoming. It is hoped that this selection of papers will not only illustrate the exciting advances presented in FPL over the last 25 years, they will also help to inspire the next generation of researchers and industrialists who will continue to send their best papers to FPL in the next 25 years and beyond.

II. FPL Significant Paper List (1991-2014)

A. Applications and Benchmarks

1995 Russell J. Petersen, Brad L. Hutchings. *An assessment of the suitability of FPGA-based systems for use in digital signal processing* [22].

1999 Simon D. Haynes, Peter Y. K. Cheung, Wayne Luk, John Stone. *SONIC - a plug-in architecture for video processing* [13].

2000 Harald Simmler, L. Levinson, Reinhard Männer. *Multitasking on FPGA Coprocessors* [24].

2003 Chi Wai Yu, K. H. Kwong, Kin-Hong Lee, Philip Heng Wai Leong. *A Smith-Waterman Systolic Cell* [27].

2007 Jorge Guajardo, Sandeep S. Kumar, Geert Jan Schrijen, Pim Tuyls. *Physical Unclonable Functions, FPGAs and Public-Key Crypto for IP Protection* [12].

2009 Shuichi Asano, Tsutomu Maruyama, Yoshiki Yamaguchi. *Performance comparison of FPGA, GPU and CPU in image processing* [2].

2010 Brian Baldwin, Andrew Byrne, Liang Lu, Mark Hamilton, Neil Hanley, Mire O'Neill, William P. Marnane. *FPGA Implementations of the Round Two SHA-3 Candidates* [3].

2013 Lin Gan, Haohuan Fu, Wayne Luk, Chao Yang, Wei Xue, Xiaomeng Huang, Youhui Zhang, Guangwen Yang. *Accelerating Solvers for Global Atmospheric Equations Through Mixed-Precision Data Flow Engine* [9].

B. Architecture

1996 C. Ebeling, D.C. Cronquist, P. Franklin. *RaPiD - reconfigurable pipelined datapath* [7].

2000 Eylon Caspi, Michael Chu, Randy Huang, Joseph Yeh, John Wawrzynek, André DeHon. *Stream Computations Organized for Reconfigurable Execution (SCORE)* [6].

2002 Kara K. W. Poon, Andy Yan, Steven J. E. Wilton. *A Flexible Power Model for FPGAs* [23].

2003 Bingfeng Mei, Serge Vernalde, Diederik Verkest, Hugo De Man, Rudy Lauwereins. *ADRES: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix* [20].

2004 Aman Gayasen, K. Lee, Narayanan Vijaykrishnan, Mahmut T. Kandemir, Mary Jane Irwin, Tim Tuan. *A Dual-VDD Low Power FPGA Architecture* [10].

C. Design Methods and Tools

1997 Vaughn Betz, Jonathan Rose. *VPR: A new packing, placement and routing tool for FPGA research* [4].

2000 Oskar Mencer, Heiko Hübert, Martin Morf, Michael J. Flynn. *StReAm: Object-Oriented Programming of Stream Architectures Using PAM-Blox* [21].

2004 Steven J. E. Wilton, Su-Shin Ang, Wayne Luk. *The Impact of Pipelining on Energy per Operation in Field-Programmable Gate Arrays* [26].

2006 Patrick Lysaght, Brandon Blodget, Jeff Mason, Jay Young, Brendan Bridgford. *Enhanced Architectures, Design Methodologies and CAD Tools for Dynamic Reconfiguration of Xilinx FPGAs* [17].

D. Dynamic Reconfiguration

1993 Patrick Lysaght, John Dunlop. *Dynamic reconfiguration of FPGAs* [18].

1996 Gordon Brebner. *A virtual hardware operating system for the Xilinx XC6200* [5].

2003 Rolf Enzler, Christian Plessl, Marco Platzner. *Virtualizing Hardware with Multi-context Reconfigurable Arrays* [8].

2005 Heiko Kalte, Mario Porrmann. *Context Saving and Restoring for Multitasking in Reconfigurable Systems* [15].

2008 Dirk Koch, Christian Beckhoff, Jürgen Teich. *ReCoBus-Builder - A novel tool and technique to build statically and dynamically reconfigurable systems for FPGAs* [16].

2009 Jonathan Heiner, Benjamin Sellers, Michael J. Wirthlin, Jeff Kalb. *FPGA partial reconfiguration via configuration scrubbing* [14].

E. Security and Network-on-Chip

2002 Maya Gokhale, Dave Dubois, Andy Dubois, Mike Boorman, Steve Poole, Vic Hogsett. *Granidt: Towards Gigabit Rate Network Intrusion Detection Technology* [11].

2003 Théodore Marescaux, Jean-Yves Mignolet, Andrei Bartic, W. Moffat, Diederik Verkest, Serge Vernalde, Rudy Lauwereins. *Networks on Chip as Hardware Components of an OS for Reconfigurable Systems* [19].

2003 Ioannis Sourdis, Dionisios N. Pnevmatikatos. *Fast, Large-Scale String Match for a 10Gbps FPGA-Based Network Intrusion Detection System* [25].

2013 Mohamed Abdelfattah, Vaughn Betz. *The Power of Communication: Energy-Efficient NoCs for FPGAs* [1].

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