Impact of Series Resistance on Bulk CMOS Current Matching over The 5–300 K Temperature Range

Nguyen Cong Dao, Abdallah El Kass, Craig T. Jin, *Senior Member, IEEE*, and Philip H.W. Leong, *Senior Member, IEEE*

***Abstract*—This letter presents the impact of source/drain series resistance on the matching of bulk NMOS and PMOS field-effect transistor current over the 5–300 K temperature range. A new method to extract series resistance is introduced, and we show experimentally that current variations, considering series resistance, increase as temperature decreases. Moreover, we propose a new approach to calculate the current mismatch based on MOSFET parameters and series resistance. The approach predicts the current variation better than the conventional model over the examined temperatures.**

***Index Terms*—Cryogenic Electronics, Current Matching, Series Resistance, MOSFETs**

I. Introduction

Device matching is an important issue that limits the performance of analog circuits. The matching of MOSFETs has been extensively studied at room temperature [1], [2], but it has not been widely investigated over a wide range of temperature, and especially at very low temperatures. Previous works in cryogenic CMOS design showed that matching of current mirrors degrades when operated at 4.2 K compared to the matching at room temperature [3]. A brief review in [4] measured the matching properties of $0.18\mu m$ CMOS at 77 K. A comparison of matching properties of Silicon on Sapphire CMOS at room temperature and 4.2 K was presented in [5]. These works have all observed that current variations increase when temperature decreases.

In this letter, we show, for the first time, the current matching of long-channel (channel length $\geq 0.35\mu m$) bulk CMOS operating from room temperature down to 5 K. A new approach for source/drain series resistance extraction, intended for performing analysis at different temperatures is presented. In addition, we introduce a new formula for the current mismatch based on MOSFET parameters and series resistance over the 5-300 K temperature range. The proposed model more accurately predicts the mismatch of current over the tested temperatures.

II. Experimental setup

The MOS transistors used in this study were fabricated in the Austrian MicroSystems 0.35 μm CMOS (C35) p-substrate mixed signal process. PMOS, NMOS devices were placed in four arrays, each having 64 transistors (4 x 16) with W = 10 μm, L = 0.35, 1, 5, and 10 μm. Devices were measured using a Keysight B1500A semiconductor analyzer. The test chip was mounted in a Closed Cycle Refrigerator-based (CCR) cryogenic probe station (LakeShore CRX-4K) fitted with temperature controllers (LakeShore TC336). A dilution refrigerator (Leiden Cryogenics CF450) was used for the measurements at 5 K. Id-Vg curves were taken at a fixed Vds of 0.1 V.

N.C. Dao, A.El Kass, C.T. Jin and P.H.W Leong are with the School of Electrical and Information Engineering, The University of Sydney, NSW, Australia. E-mail: nguyen.dao@sydney.edu.au.

III. Parameter extractions

The approach used to obtain threshold voltage, V_{th}, was presented in [6]. For mobility, μ, and source-drain series resistance, R_{sd}, over the examined temperatures, we used the drain current model in [7]. As temperature changes, the contact resistance, resistance of the source/drain diffusion, and the channel length reduction, ΔL, vary significantly. Conventional methods failed to accurately extract series resistance [8]. Moreover, unlike existing methods which assume R_{sd} to be constant or have gate voltage dependence [9]–[12], we consider R_{sd} and ΔL as being channel length and gate voltage dependent [13]–[15]. Since R_{sd} and ΔL are interdependent, it is very difficult to separate their contributions in the total resistance from different channel lengths when gate voltage varies. However, based on the aforementioned analysis, we assume that R_{sd} can be split into two components: R_{sd0}, the series resistance which is independent of channel length variations due to overdrive gate voltage, V_{gst}=V_{gs}-V_{th}, and R_{sdL} which denotes variations of the series resistance to channel lengths and V_{gst}. Both R_{sd0} and R_{sdL} are functions of temperature.

Using a set of same width devices, different lengths (i.e. L_1, L_2), the channel resistance and the series resistance can be extracted via the total channel resistance R_{tot} as follows

$$\begin{aligned} R_{tot} &= \frac{V_{ds}}{I_{ds}} = R_{ch0}L + R_{sd0} + R_{sdL} \\ R_{tot,L_{12}} &= R_{ch0}L_{12} + R_{sdL1} - R_{sdL2}, \end{aligned} \tag{1}$$

where L is the mask length, L_{12} = L_1 - L_2, and R_{ch0} is normalised intrinsic channel resistance per unit length,

$$R_{ch0} = \frac{1 + (\theta V_{gst})^{n-1}}{\mu_g C_{ox} W \theta^{n-2} V_{gst}^{n-1}}, \tag{2}$$

where μ_g is a generalised mobility, θ is the mobility attenuation factor, and n is an exponent factor [7].

For long (L1) and short (L2) channel devices, we can assume that $R_{tot,L12} \approx R_{ch0}L_{12} \gg R_{sdL1}$ - R_{sdL2}. Then, $R_{ch0} \approx \frac{R_{tot,L_{12}}}{L_{12}}$ ($\Omega/\mu m$). Another assumption for a long channel device L_1 is $R_{tot,L1} \approx R_{ch0}L_1$ + $R_{sd0} \gg R_{sdL1}$.

Therefore, $R_{sd0} \approx R_{tot,L_1}$ - $R_{ch0}L_1$, and R_{sdL} can be obtained from R_{tot} (Eq. (1)).

The intrinsic MOSFET parameters, μ_g and θ, can be extracted from R_{ch0} (Eq. (2)). The coefficients from the best fitted R_{ch0} versus V_{gst} while varying n (from 2 to 3) and temperatures reveal the value of n and θ. μ_g can be obtained from R_{ch0} after n and θ are determined. The effective mobility, μ_{eff}, is calculated as [7]

$$\mu_{eff} = \mu_g \frac{(\theta V_{gst})^{n-2}}{1+(\theta V_{gst})^{n-1}}. \tag{3}$$

The mismatch of current (ΔI_d), parameters (ΔV_{th}), ($\Delta\mu$), and series resistance (ΔR_{sd}) were obtained from two adjacent transistors. The distance between two adjacent transistors is about $2\mu m$. For each transistor size, 96 pairs were used in this study.

IV. MOS Matching Model

The common current matching model for a pair of transistors, considering impact of series resistance, is given in [9]

$$\sigma^2_{\left(\frac{\Delta I_d}{I_d}\right)} = \left(\frac{g_m}{I_d}\right)^2 \sigma^2_{(\Delta V_{th})} + (1-G_d R_{sd})^2 \sigma^2_{\left(\frac{\Delta\mu}{\mu}\right)} + G_d^2 \sigma^2_{(\Delta R_{sd})}, \tag{4}$$

where g_m is the transconductance, and G_d is the channel conductance. In Eq. (4), the correlations between V_{th}, μ, and R_{sd} fluctuations are considered negligible as R_{sd} is assumed constant. This model is accurate for devices operating in the strong inversion region at room temperature [16]. For a wide range of temperatures, since the channel resistance R_{ch} and series resistance R_{sd} vary significantly with the gate voltage and temperature, the correlation between series resistance and channel resistance must be taken into account. Based on the current model $I_d = V_d/(R_{ch} + R_{sd})$, the current variation, departing from first order Taylor approximation, can be obtained as

$$\begin{aligned}\sigma^2_{\left(\frac{\Delta I_d}{I_d}\right)} &= \left(\frac{1}{I_d}\frac{\partial I_d}{\partial R_{ch}}\right)^2 \sigma^2_{\Delta R_{ch}} + \left(\frac{1}{I_d}\frac{\partial I_d}{\partial R_{sd}}\right)^2 \sigma^2_{\Delta R_{sd}} \\ &\quad + 2\frac{1}{I_d^2}\frac{\partial I_d}{\partial R_{ch}}\frac{\partial I_d}{\partial R_{sd}} \rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}} \\ &= G_d^2\left(\sigma^2_{\Delta R_{ch}} + \sigma^2_{\Delta R_{sd}} + 2\rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}}\right),\end{aligned} \tag{5}$$

where $\rho_{(\Delta R_{ch},\Delta R_{sd})}$ is the correlation between R_{ch} and R_{sd}.

The variability $\sigma_{\Delta R_{ch}}$ can be rewritten in terms of $\sigma_{\Delta V_{th}}$ and $\sigma_{\Delta\mu/\mu}$ as follows

$$\begin{aligned}\sigma^2_{\Delta R_{ch}} &= \left(\frac{\partial R_{ch}}{\partial \mu}\right)^2 \sigma^2_{\Delta\mu} + \left(\frac{\partial R_{ch}}{\partial V_{th}}\right)^2 \sigma^2_{\Delta V_{th}} \\ &= \frac{1}{G_d^2}\left((1-G_d R_{sd})^2 \sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_d}\right)^2 \sigma^2_{V_{th}}\right).\end{aligned} \tag{6}$$

It is worth noting that the correlation between μ and V_{th} can be negligible. Replace Eq. (6) into Eq. (5), the current matching model becomes

$$\begin{aligned}\sigma^2_{\left(\frac{\Delta I_d}{I_d}\right)} &= (1-G_d R_{sd})^2 \sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_d}\right)^2 \sigma^2_{V_{th}} \\ &\quad + G_d^2 \sigma^2_{\Delta R_{sd}} + 2G_d^2 \rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}}.\end{aligned} \tag{7}$$

V. Results and Discussions

Results of series resistance extraction for NMOS are shown in Fig. 1. It can be seen that Eq. (1) fits the measured data better than the existing method, which deviates from the measurements, mostly at low V_{gst} and low temperatures. Here, the conventional extraction method [17], used in comparison, assumes that ΔL is a constant and R_{sd} is a function of V_{gst}. For both NMOS and PMOS, our extraction approach and the existing method are similar at room temperature but the old method loses its accuracy with decreasing temperature. In this approach, mobility is assumed as channel length independent since channel length greater 100 nm [18]. Therefore, the validation of this approach mainly depends on the error in the R_{ch0} approximation. Our empirical results (Fig. 2) suggest that, L_{12} should be greater than 5 μm and $V_{gst} > 0.5$ V for the best extraction results. Repeatable results can be obtained since the difference between R_{sd} extracted from linear regression when using several gate-mask-length and from long-short (i.e. L_{12} = 9 μm) pair devices is very small (less than 3.1%).

Mobility and its attenuation factor are calculated from the best fitting coefficients of R_{ch0} (Eq. (2)). It is worth noting that to keep the physical meaning of n [19], its fitting boundaries are referenced from [7]. The maximum fitting error (adjusted R-squared) is less than 0.3% for all type of transistors over the 5-300 K temperature range. Mobility at room temperature, μ_g=376 cm^2/Vs (NMOS) and μ_g=123 cm^2/Vs (PMOS), are very close to the values from foundry (370 and 126, respectively). At 100 K, the effective mobility extracted from our approach and from [17] show similar results for the same device size (about 1500 cm^2/Vs in NMOS and 300 cm^2/Vs in PMOS).

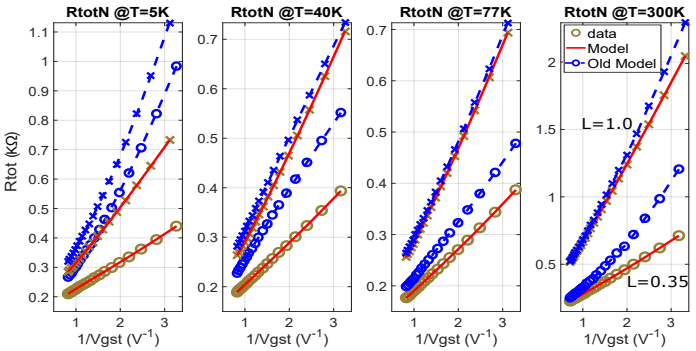

Fig. 1. The total resistance of NMOS W = 10 μm, L = 1, 0.35 μm: measured data (symbols), new extraction (lines), and conventional extraction (dashed symbol lines).

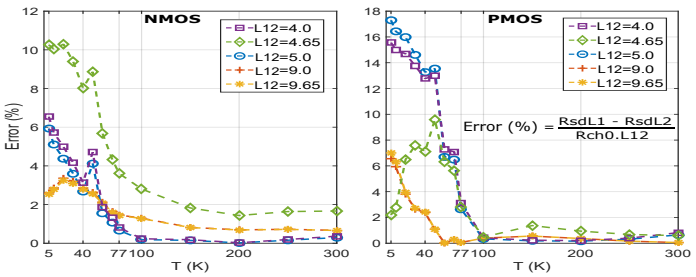

Fig. 2. Error in R_{ch0} approximation at V_{gst} = 1V.

Current mismatch of NMOS and PMOS versus our model (Eq. (7)) and the conventional model, (Eq. (4)), from 5 K to 300 K are plotted in Fig. 3.

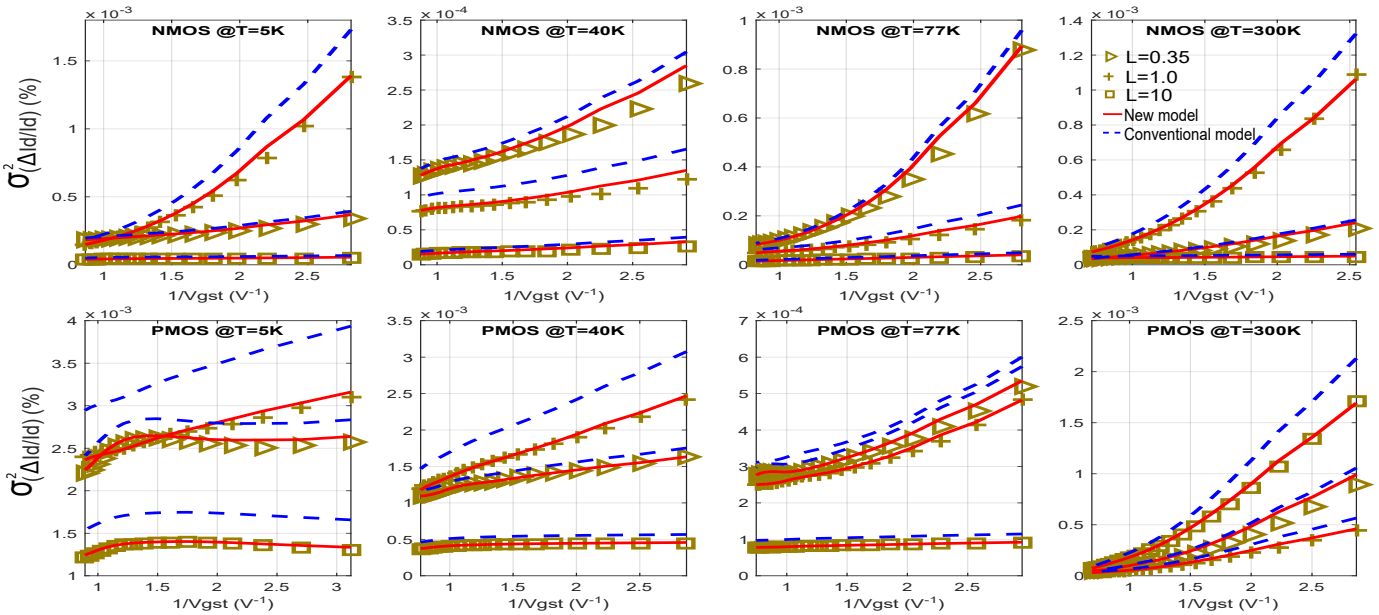

Fig. 3. Current variation of NMOS, PMOS W=10μm, L=10, 1, 0.35μm: data (symbol) vs. proposed model (solid line) and conventional model (dash line)

TABLE I
COMPARISON BETWEEN EXPERIMENTAL DATA VS. OUR MODEL AND CONVENTIONAL MODEL AT V_{gst} = 1V
(ERROR (%) = $100\frac{|\sigma_{\Delta I_d/I_d,Model}-\sigma_{\Delta I_d/I_d,data}|}{\sigma_{\Delta I_d/I_d,data}}$)

T (K)	5	40	77	100	200	300
NMOS W/L = 10/0.35						
Our model (%)	0.72	0.67	0.47	1.08	1.24	2.26
Rahhal's model (%)	4.42	4.36	4.13	4.74	4.89	5.89
PMOS W/L = 10/0.35						
Our model (%)	0.87	0.06	0.20	0.20	1.31	3.55
Rahhal's model (%)	4.59	3.62	3.88	3.88	4.95	7.11

At room temperature, our model and the existing model have similar results in strong inversion (V_{gst} = 1V) for both PMOS and NMOS devices. However, the accuracy of the existing model declines at low temperatures, especially for short channel devices. Taking into account the correlation between channel resistance and series resistance helps our model fit to the experimental data from 300 K down to 5 K. Comparison between our model and the existing model for short channel devices are given in Table I.

TABLE II
SUMMARY OF RESULTS AT V_{gst} = 1 V

T (K)	5	40	77	100	200	300
NMOS W/L = 10/0.35						
$\sigma_{\Delta V_{th}}$ (mV)	5.07	5.09	5.09	5.01	4.50	4.35
$\sigma_{\Delta\mu/\mu}$ @V_{gst} (%)	0.33	0.26	0.17	0.11	0.06	0.04
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{gst} (%)	1.69	1.45	1.31	1.11	1.78	2.44
$\sigma_{\Delta I_d/I_d}$ @V_{gst} (%)	1.38	1.17	0.99	0.79	0.85	0.70
PMOS W/L = 10/0.35						
$\sigma_{\Delta V_{th}}$ (mV)	4.00	4.42	3.95	4.42	6.75	7.98
$\sigma_{\Delta\mu/\mu}$ @V_{gst} (%)	3.53	1.52	0.39	0.22	0.08	0.06
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{gst} (%)	5.31	3.92	2.04	1.79	2.14	2.32
$\sigma_{\Delta I_d/I_d}$ @V_{gst} (%)	4.48	3.48	1.67	1.35	1.10	0.96

Variations of threshold voltage, mobility, series resistance and the current at V_{gst} = 1 V are shown in the Table II. It can be seen that most parameter factors increase as temperature decreases, i.e. current matching degrades at low temperatures. Noting that the current magnitude increases with decreasing temperature, normalised current variations over the studied temperatures are shown in Fig. 4. In general, the current variations in both PMOS and NMOS transistors change slightly from 300 K down to 100 K, and then increase more dramatically as temperature further decreases. An explanation for this increased variation at cryogenic temperatures is due to the freeze-out of carriers which strongly impacts on the effective dopant concentrations and the carrier mobility.

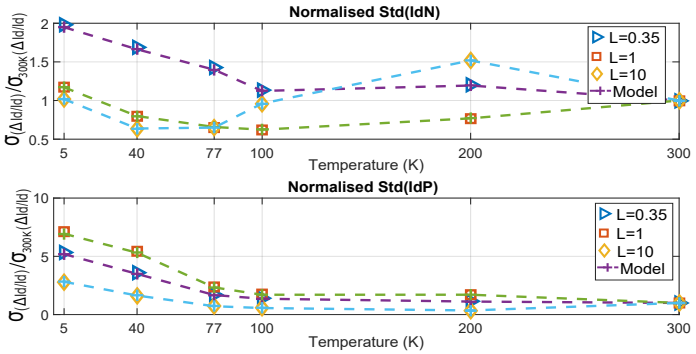

Fig. 4. Normalised Current variations at V_{gst} = 1 V: data (symbol) and model (dash line)

VI. CONCLUSION

We presented the impact of source/drain series resistance on current matching for long-channel bulk CMOS transistors at room temperature down to 5 K. An approach to extract series resistance was introduced and verified. A new formula to calculate current mismatch, considering series resistance, is also proposed. Our model is simply yet reliable, making it suitable for bulk CMOS characterisation and circuit evaluation over a wide range of temperature. Future work will involve validating this approach on nanometer scale transistors.

ACKNOWLEDGMENT

The authors would like to thank Y. Yang, K. Das, and Prof. D. Reilly for their support in chip measurements. This work was supported by the University of Sydney, Australian Institute for Nanoscale Science and Technology Accelerator Scheme.

REFERENCES

[1] P. Andricciola and H. P. Tuinhout, "The temperature dependence of mismatch in deep-submicrometer bulk MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 690–692, 2009, DOI:10.1109/LED.2009.2020524.

[2] J. A. Croon, W. M. Sansen, and H. E. Maes, *Matching properties of deep sub-micron MOS transistors*. Springer, 2005.

[3] M. T. Rahman and T. Lehmann, "A cryogenic D/A converter with novel charge injection reduction technique for silicon quantum computer controller circuit," in *2010 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. IEEE, 2010, pp. 1151–1154, DOI:10.1109/APCCAS.2010.5774978.

[4] P. Martin, A. Royet, F. Guellec, and G. Ghibaudo, "MOSFET modeling for design of ultra high performance infrared CMOS imagers working at cryogenic temperature: Case of analog/digital 0.18 μm CMOS process," *Solid-State Electronics*, vol. 62, no. 1, pp. 115–122, 2011, DOI:10.1016/j.sse.2011.01.004.

[5] K. Das and T. Lehmann, "Effect of deep cryogenic temperature on silicon-on-insulator CMOS mismatch: A circuit designers perspective," *Cryogenics*, vol. 62, pp. 84–93, 2014, DOI:10.1016/j.cryogenics.2014.04.014.

[6] N. C. Dao, A. El Kass, M. R. Azghadi, C. T. Jin, J. Scott, and P. H. Leong, "An enhanced MOSFET threshold voltage model for the 6–300K temperature range," *Microelectronics Reliability*, vol. 69, pp. 36–39, 2016, DOI:10.1016/j.microrel.2016.12.007.

[7] A. Emrani, F. Balestra, and G. Ghibaudo, "Generalized mobility law for drain current modeling in Si MOS transistors from liquid helium to room temperatures," *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 564–569, 1993, DOI:10.1109/16.199361.

[8] A. Ortiz-Conde, A. Sucre-González, F. Zárate-Rincón, R. Torres-Torres, R. S. Murphy-Arteaga, J. J. Liou, and F. J. García-Sánchez, "A review of DC extraction methods for MOSFET series resistance and mobility degradation model parameters," *Microelectronics Reliability*, 2017, DOI:10.1016/j.microrel.2016.12.016.

[9] L. Rahhal, A. Bajolet, C. Diouf, A. Cros, J. Rosa, N. Planes, and G. Ghibaudo, "New methodology for drain current local variability characterization using Y function method," in *2013 IEEE International Conference on Microelectronic Test Structures (ICMTS)*. IEEE, 2013, pp. 99–103, DOI:10.1109/ICMTS.2013.6528153.

[10] D. Fleury, A. Cros, G. Bidal, J. Rosa, and G. Ghibaudo, "A new technique to extract the source/drain series resistance of MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 975–977, 2009, DOI:10.1109/LED.2009.2026592.

[11] J. Henry, Q. Rafhay, A. Cros, and G. Ghibaudo, "New Y-function based MOSFET parameter extraction method from weak to strong inversion range," *Solid-State Electronics*, vol. 123, pp. 84–88, 2016, DOI:10.1016/j.sse.2016.06.004.

[12] A. Karsenty and A. Chelly, "Y-function analysis of the low temperature behavior of ultrathin film fd soi mosfets," *Active and Passive Electronic Components*, vol. 2014, 2014, DOI:10.1155/2014/697369.

[13] J. Kim, J. Lee, I. Song, Y. Yun, J. D. Lee, B.-G. Park, and H. Shin, "Accurate extraction of effective channel length and source/drain series resistance in ultrashort-channel MOSFETs by iteration method," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2779–2784, 2008, DOI:10.1109/TED.2008.2003081.

[14] M. Joodaki, "On the extraction of the external drain and source resistors and effective channel length in Si-MOSFET," *Solid-State Electronics*, vol. 111, pp. 1–6, 2015, DOI:10.1016/j.sse.2015.04.005.

[15] J. Campbell, K. Cheung, S. Drozdov, R. Southwick, J. Ryan, A. Oates, and J. Suehle, "Channel length-dependent series resistance?" in *Silicon Nanoelectronics Workshop (SNW), 2012 IEEE*. IEEE, 2012, pp. 1–2, DOI:10.1109/SNW.2012.6243299.

[16] E. Ioannidis, C. Theodorou, S. Haendler, E. Josse, C. Dimitriadis, and G. Ghibaudo, "Impact of source–drain series resistance on drain current mismatch in advanced fully depleted SOI n-MOSFETs," *IEEE Electron Device Letters*, vol. 36, no. 5, pp. 433–435, 2015, DOI:10.1109/LED.2015.2411289.

[17] G. Niu, J. D. Cressler, S. J. Mathew, and S. Subbanna, "A total resistance slope-based effective channel mobility extraction method for deep submicrometer CMOS technology," *IEEE Transactions on Electron Devices*, vol. 46, no. 9, pp. 1912–1914, 1999, DOI:10.1109/16.784194.

[18] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez *et al.*, "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling," in *Electron Devices Meeting, 2006. IEDM'06. International*. IEEE, 2006, pp. 1–4, DOI:10.1109/IEDM.2006.346872.

[19] F. Balestra, L. Hafez, and G. Ghibaudo, "A new method for the extraction of MOSFET parameters at ambient and liquid helium temperatures," *Le Journal de Physique Colloques*, vol. 49, no. C4, pp. C4–817, 1988, DOI:10.1051/jphyscol:19884172.