Implementation of Gabor-type Filters on Field Programmable Gate Arrays

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Abstract

Although biological visual systems have been widely studied at the physiological, psychophysical and functional levels, our understanding of its signal processing mechanisms is still very rudimentary. One of the obstacles in this process is the difficulty of dealing with the vast amounts of processing necessary to test real-time temporal models of the visual system. In this paper, we first present a high performance FPGA-based cellular neural network which implements a Gabor-type filter. This is a building block element which we intend to use with different parameters to model cells in V1. The application of the Gabor-type filter in a neuromorphic system consisting of an analog VLSI retina chip interfaced to our Gabor chip is also presented. The retina chip serves as an imager and transmits its output to the FPGA via an address event representation (AER) transceiver [1]. Using AER, multiple chips can be interconnected in a modular network to form large networks of Gabor chips. By combining both analog VLSI chips and digital chips (e.g. DSP chips, microprocessors, and FPGA chips), we hope to make real-time implementations of early vision models and visualize their temporal behaviour, while achieving a level of performance, integration, power consumption, area and flexibility not possible using any technology in isolation.

1. Implementation

A Gabor filter can be represented by the complex valued convolutional kernel $g(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} e^{j(\omega_x x+\omega_y y)}$ [4] where $\sigma, \omega_x, \omega_y$ are real constants. The even kernel is cosine modulated and the odd kernel is sine modulated and hence two filers are 90 degrees out of phase. Pollen and Ronner suggested that adjacent neurons in visual cortex have even and odd symmetry [5] and therefore Gabor-filters can model receptive field profiles in the visual cortex [3]. Cellular neural networks (CNN) can be used to implement Gabor-type filters [6].

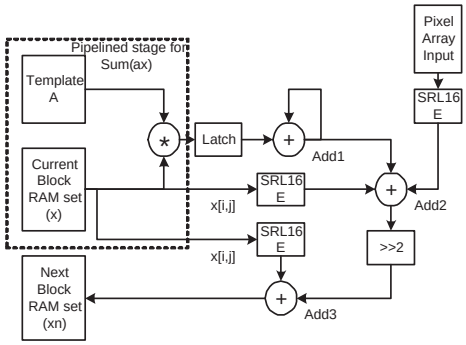

Figure 1. Architecture of Euler core

Let u_{ij}, x_{ij} and y_{ij} represent the input, state and output pixels of an image respectively. The dynamics of the CNN are governed by the differential equation

$$\tau \frac{dx_{ij}}{dt} = f_{ij} = -x_{ij} + \sum_{kl \in N_r} a_{kl} y_{kl} + \sum_{kl \in N_r} b_{kl} u_{kl} \quad (1)$$

where a_{kl} represents the feedback template and b_{kl} represents the control template. By changing the values of the templates, the Gabor-type filter can be tuned to respond to different orientations, bandwidth and spatial scales.

The approach used in our FPGA implementation of the Gabor-type filter was to develop a pipelined datapath which can perform the required complex multiply accumulate operations for the solution of Equation 1 using Euler's method. Inputs, templates and outputs are stored in internal memories of the FPGA so that the coefficients that control orientation and spatial scale are easily adjusted. A single core can process data in a time multiplexed manner with different parameters. Multiple cores can be also used to increase performance.

Gabor-type filters have a complex valued convolutional kernel, and a data format with complex values is used. As fixed-point arithmetic implementations require less area, two's complement fractions are used. A core is built based

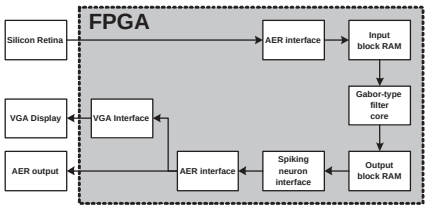

Figure 2. Architecture of silicon retina system

on 16-bit fixed-point arithmetic and the Euler integration method. The data format consists of two 16-bit words which are used for the even and odd kernels of equation 1. The 16-bit words consist of a 4-bit integer part and 12-bit fractional part. For the VGA interface, image pixels are represented by an 8-bit number.

Our Gabor-type filter is used as the processing unit in a silicon retina system as shown in figure 2. In the system, a silicon retina, leaky integrators, Gabor-type filter core, and spike generator are integrated. The silicon retina is a custom designed analog VLSI chip [7] and the other components are implemented on an FPGA.

2. Results

In [2], Choi et. al. presented an analog VLSI retina system with a Gabor-type filter VLSI chip. Our FPGA-based Gabor-type filters are fully compatible with this system since both chips use the same AER input/output format. The Euler core was implemented using VHDL on a Celoxica RC200 platform which is populated with a Xilinx XC2V1000-4. For 1024 pixel frames, our entire implementation uses 1962 slices, operates at 120 MHz and achieves 23,000 Euler iterations over one frame per second.

The power consumption of the analog Gabor chip ($0.25\mu m$ technology at $2.5 - 3\ V$) and its peripherals as described in [2] is $44.1mW$. The power consumption of the FPGA chip ($0.12\mu m$ technology at $1.5\ V$) and all the peripherals on the RC200 platform in the reset state is $1.929W$. This increases to $1.946W$ when the Euler core is processing.

A ring pattern in black with a white background is displayed on a LCD monitor and captured using the silicon retina. The image is processed by the FPGA-based Gabor-type filter processor using templates corresponding to different orientations. Results are shown in figure 3

3. Conclusion

An implementation of Gabor-type Filters on field programmable gate arrays using cellular neural network (CNN) architecture is described. Compared to other analog VLSI implementations of Gabor-type filters, our implementation has advantages of shorter design time, scalability and flexibility. The design can accommodate different array sizes, as well as simultaneous computation of multiple filter outputs tuned to different orientations and bandwidths.

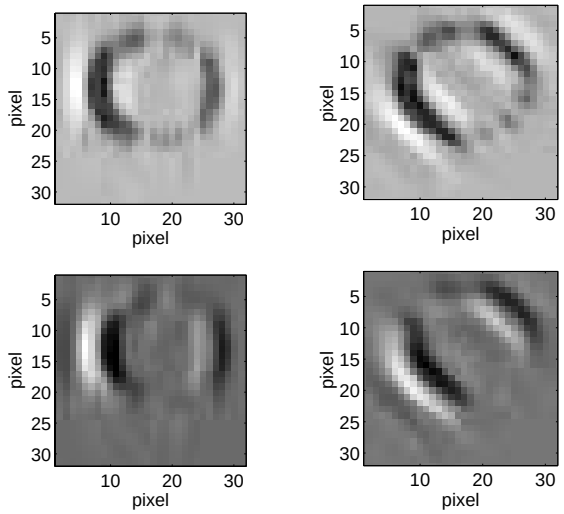

Figure 3. Odd (upper) and even (bottom) output for ring pattern input with vertical (left) and 45 degree (right) orientations.

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