CHARACTERISATION AND MODELLING OF BULK CMOS TRANSISTORS OVER THE 5-300 K TEMPERATURE RANGE

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To my parents, for their sacrifices and love.

Abstract

With the increasing interest in MOSFET device operation in extremely cold environments, circuit designs for low-temperature applications have attracted recent attention. Device characterisation and modelling are crucial steps in circuit designs, and an appropriate approach for transistor characterisation at cryogenic temperatures is required to provide insight into transistor behaviour, and to develop reliable models for circuit simulations over the required operating temperatures.

This work presents a detailed study of bulk CMOS transistors behaviour from room temperature down to 5 K. A new approach to extract intrinsic and extrinsic parameters of bulk CMOS over a wide range of temperature is proposed. Extracted MOSFET parameters reveal changing characteristics over the examined temperatures. Transistor characteristics are modelled based on physical properties of device and empirical results. This thesis introduces an enhanced MOSFET threshold model, based on a simplified Fermi potential and a field-assisted ionisation, derived from physics and experimental data. The model predicts the threshold voltage better than the conventional model, especially at low temperatures. An adapted carrier mobility model derived from a conventional model is experimentally verified. This work also presents a Verilog-A SPICE model based on the proposed models and extraction results. The SPICE model can be incorporated into Cadence Spectre simulator for circuit simulations at low temperatures. The SPICE model can replicate the I-V characteristics of the bulk CMOS over a wide temperature range.

The matching of transistors is one of the most important aspects of high performance integrated circuit design. Results from this research reveal, for the first time, the matching properties of MOSFETs and its parameters over the 5-300 K temperature range. In addition, a new formula to calculate the current matching in bulk CMOS devices based on the threshold voltage, mobility and series resistance is introduced. The proposed formula obtained better results compared to the existing formula at low

temperatures. The effects of device geometries on MOSFET parameter matching and current matching are also exposed. Matching results from PMOS and NMOS devices provide a view of device parameter variations from room temperature down to 5 K.

Statement of Originality

I certify that the intellectual content of this thesis is the product of my own work and that all the assistance received in preparing this thesis and sources have been acknowledged specifically:

- The test chips were designed jointly by the author, Mr Abdallah El Kass, Dr Kushal Das, and Dr Yuanyuan Yang.
- Chip measurements were conducted at the Quantum Nanoscience Laboratory, the University of Sydney with supports from Mr Abdulla El Kass, Dr Kushal Das, and Dr Yuanyuan Yang.

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Finally, thank you God for the infinite grace showered on me.

Symbols

$C_{ox}^{'}$	Gate capacitance per unit area
ε_{Si}	Permittivity of Silicon
ε_{ox}	Permittivity of SiO_2
ε_0	Permittivity of free space
E_C	Conduction band edge
E_F	Fermi energy
E_i	Intrinsic energy level
E_D	Valence band edge
k	Boltzmann constant
N_A	Acceptor concentration
N_D	Donor concentration
N_C	Effective density of states in the conduction band for Si
N_V	Effective density of states in the valence band for Si
n	Exponent factor, which is related to characteristics of carrier scattering mechanisms
q	Magnitude of electronic charge
Φ_0	Surface potential
Φ_F	Fermi potential
Φ_{AF}	Activation potential
γ	Body bias coefficient
R_{tot}	Total channel resistance
R_{ch}	Channel resistance
R_{ch0}	Channel resistance per unit length
R_{sd}	Source/Drain series resistance
R_{sd0}	Channel length independence Source/Drain series resistance
R_{sdL}	Channel length dependence Source/Drain series resistance
g_m	Transconductance

$Q_0^{'}$	Effective oxide charge per unit area
Q_B	Depletion region charge
Q_I	Inversion layer charge
$1/S$	Subthreshold slope
T_{ox}	Oxide thickness
T	Absolute temperature
θ	Mobility attenuation factor
μ	Effective mobility
μ_m	Maximum mobility
V_{T0}	Threshold voltage of long channel
V_T	Threshold voltage

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ADE	Analog Design Environment
AMS	Austrian MicroSystem
ASIC	Application Specific Integrated Circuit
AWG	Arbitrary Waveform Generator
BJT	Bipolar Junction Transistor
CCR	Closed Cycle Refrigerator
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
EKV	Enz-Krummenacher-Vittoz
FD-SOI	Fully Depleted Silicon-On-Insulator
FS-SOS	Fully Depleted Silicon-On-Sapphire
HiSIM	Hiroshima University Semiconductor Technology Academic Research Center IGFET
IC	Integrated Circuit
IGFET	Insulated Gate Field Effect Transistor
I-V	Current-Voltage
LDD	Lightly Doped Drain
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Complementary Metal Oxide Semiconductor
PCB	Printed Circuit Board
PMOS	P-type Complementary Metal Oxide Semiconductor
PSP	Surface potential-Based MOSFET
Qubits	Quantum bits
RF	Radio Frequency
SPICE	Simulation Program with Integrated Circuit Emphasis

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Chapter 1

Introduction

1.1 Motivation and Approach

Quantum computing has recently attracted great interest since it promises unprecedented computational ability. Apart from the arrays of quantum bits (qubits), acting as the fundamental elements in the quantum system, a key subsystem of all quantum computers is the interface between the isolated qubits and classical control and readout circuitries needed to govern the system [1,2]. The qubits have to operate at nearly absolute zero (milli-Kevin) to suppress errors due to thermal excitation [3,4]. To realise quantum machinery operating at very low temperature, integrated circuits are deployed in the interface circuit [5,6]. Using standard Complementary Metal-Oxide-Semiconductor (CMOS) to implement such control/interface circuits, close proximity to qubits is preferable as parasitic effects, such as cable capacitance and inductance, can be minimised and enhance circuit performance [7,8]. It is well known that CMOS devices working at low temperatures perform better compared to that at room temperature in term of speed and power dissipation, due to improved carrier mobility, sub-threshold slope, and better latch-up immunity [9,10]. However, some abnormal behaviours of the devices, caused by cryogenic effects, such as carriers freeze-out, kink effect or hysteresis, result in the unreliability of the circuit thus affecting its performance [11–13].

Since the introduction of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [14], its characteristics have been extensively studied, revealing detailed properties regarding its operation, and making it possible to model its operation mathematically and simulate its behaviour. Circuits designed for the low-temperature applications base on room temperature models may have degraded performance or not work at all [15]. Some MOSFET models for low-temperature circuit evaluation, i.e. at 77 K [16, 17] or at 20 K [18], have been reported and applied for space applications. These models either used polynomial fitting functions or

modified from room temperature models might not provide insight into the device behaviour, consequently, they cannot reuse for different technologies. Due to a lack of appropriate models for bulk CMOS operating at deep cryogenic temperatures, characterisation and modelling of CMOS at these low temperatures is important to reveal device insights and provide reliable means to developing quantum interface circuits.

The objectives of this work are to extensively study bulk CMOS characteristics and model its operations from room temperature down to liquid helium temperature (4.2 K). For the work conducted in this thesis, full-custom test chips, including thousands of transistors, were fabricated and measured at different temperatures ranging from 300 K down to 5 K. In this work, the actual temperature value recorded by a thermometer when measuring test chips at 4.2 K stage in the dilution refrigerator was about 5 K. Current-voltage characteristics, including drain current versus gate voltage (I_D - V_{GS}), drain current versus drain voltage (I_D - V_{DS}), are taken, extracted, then analysed using Matlab. Models derived from physics and experimental data were incorporated into Spectre simulator (Cadence) and verified against the measured data. The experiment was conducted at the Quantum Nanoscience Laboratory, The University of Sydney.

1.2 Contributions

This dissertation extensively studies bulk CMOS characteristics and its operation over the 5 - 300 K temperature range. The original contributions presented throughout this thesis can be itemised as below:

- This presents a new approach to extract source/drain series resistance and MOSFET parameters from room temperature down to liquid helium temperature. This technique can overcome limitations from existing extraction techniques [19]. The approach considers carrier mobility to be channel length independent while the source/drain series resistance is channel length dependent. This work was the first to evaluate and validate this approach in bulk 0.35 μm CMOS at very low temperatures [20].

- A novel threshold voltage model of bulk CMOS operating over a wide range of temperatures. This enhanced model is derived from physics including effects of freeze-out carriers at very low temperatures. The proposed model is simple, making it suitable for hand calculation and it is accurate for short channel devices [21].

- A new compact Simulation Program with Integrated Circuit Emphasis (SPICE) [22] model of bulk CMOS for cryogenic circuit simulation is introduced. The model is derived from the Berkeley Short-channel IGFET Model (BSIM) [23] with the modified threshold voltage and mobility model for the 5 - 300 K temperature range. It was developed

using the Verilog-A language and tested in the Cadence Spectre simulator. This compact Verilog-A model describes current-voltage characteristics of MOS transistor operating in the strong inversion region.

- For the first time, matching properties of bulk CMOS NMOS and PMOS transistor extracted from thousands of transistors from room temperature down to liquid helium temperature are presented. Impacts of temperature and device geometries on the matching are discussed thoroughly. In addition, a new formula to calculate the mismatch of current pairs applied for all temperatures is proposed. The proposed current mismatch formula fits better than existing models, especially at cryogenic temperatures. This study and proposed formula are very useful for circuit analysis and design for low-temperature applications [20].

1.3 Thesis Structure

This dissertation is arranged in seven chapters. Following this introductory chapter, a detailed review on CMOS characteristics at low temperatures is given. Thus Chapter 2 summarises most of the aspects of CMOS related to parameters, operations, and reliability when temperature changes from literature.

Chapter 3 begins with a review of parameter extraction methods for MOS transistors. Discussions of limitations of existing methods at cryogenic temperatures are given. Next, a new approach in characterising source/drain series resistance and parameter extraction for bulk CMOS over the 5 - 300 K temperature range is introduced. Detailed extraction results such as threshold voltage, mobility, mobility attenuation factor or source/drain series resistance are then demonstrated.

Chapter 4 provides detailed background theory relating to the threshold voltage of the MOSFETs. The proposed threshold voltage model is then presented, followed by descriptions of short channel effects. Explanation and further discussions on results from our semi-empirical models are then added in the last section of this chapter.

Chapter 5 begins with introductions of temperature dependent models for carrier mobility, series resistance, and a compact I-V model. Description of the cryogenic SPICE compact I-V model is then briefly summarised. Comparison results between the proposed model and the measurements are provided, accompanied with discussions on improvements as well as limitations of the proposed SPICE model.

Chapter 6 covers all of the matching properties of bulk CMOS from 5 K to 300 K. It starts with a brief review on impacts of temperature on the matching of MOS transistors. Following

the discussion about existing matching models, a new formula in calculating mismatch of the currents applied to a wide range of temperature is presented. The temperature effect on the mismatch of bulk CMOS parameters is also thoroughly explained and discussed.

In the final chapter, a summary of the work in this thesis and directions for future works are presented.

Chapter 2

Low temperature CMOS

This chapter reviews bulk CMOS characteristics and their operation at low temperatures. The chapter begins with a background theory of impurity ionisation, carrier channel formation, and a brief summary of MOS operations. In the next section, a review on MOSFET parameter variabilities over a wide range of temperature is presented. Summaries of influences of impurity freeze out and some abnormal behaviours of MOS devices at cryogenic temperatures, are then provided. Finally, the reliability of CMOS devices and circuits at cryogenic temperatures are discussed.

2.1 MOS operations at cryogenic temperatures

2.1.1 Dopant ionisation

2.1.1.1 Impurity ionisation

The operation of MOS devices can be explored by examining impurity ionisation, dopant concentrations and the transport of carrier currents (holes, electrons) in the channel. Studies of impurity ionisation and current transport in solid devices have been extensively documented [14, 24].

When a certain impurity is introduced in the semiconductor, the impurity energy level is added to the energy band diagram. In conventional MOS devices, the silicon substrate is doped with phosphorous donors (N_D) and boron acceptors (N_A) atoms with energy levels allocated at about 0.045 eV from the corresponding band edge [14]. Figure 2.1 presents the schematic energy band of doped semiconductors with donor ions and acceptor ions, where E_C, E_V and E_i denote energy levels of the conduction band, the valence band and the intrinsic energy, respectively.

At room temperature, a small difference in energy between the doping level and the corresponding bands, conduction band for electrons, and valence band for holes, allows carriers to be easily excited into the band, leaving behind ionised impurities [9, 14].

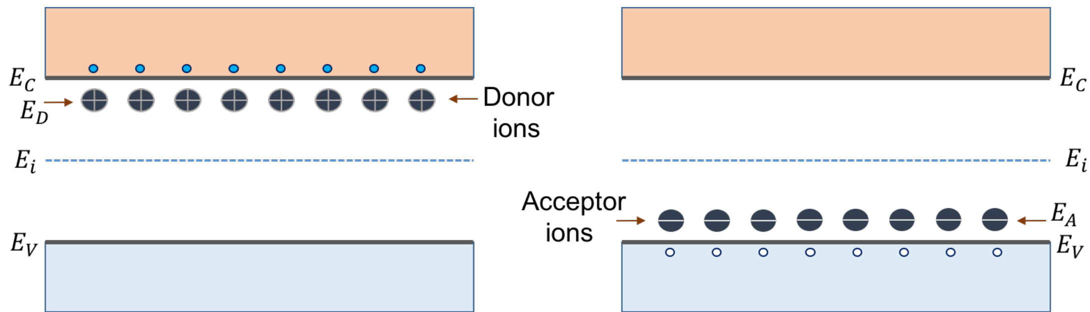


Figure 2.1: Schematic energy band of doped semiconductor (adapted from [14]).

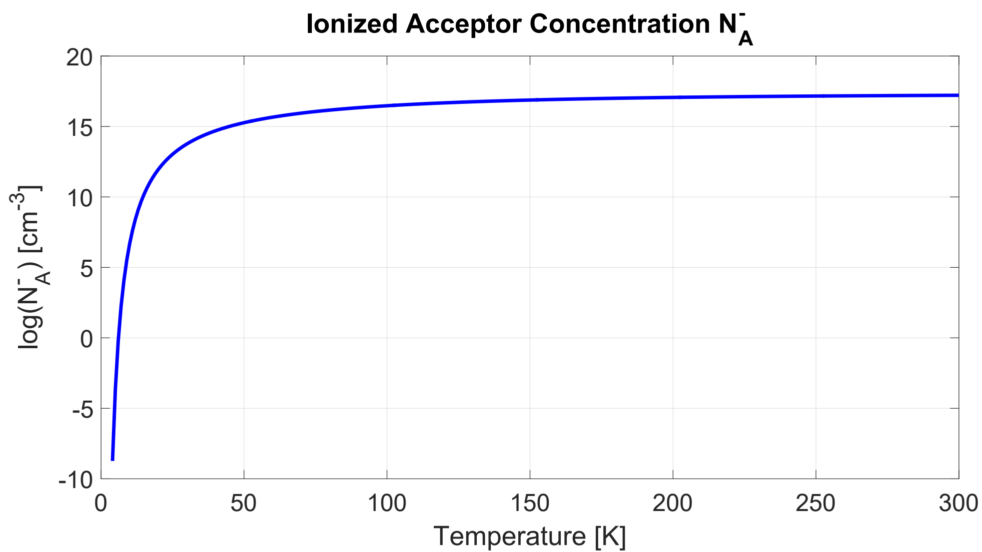


Figure 2.2: Impact of temperature on ionised acceptor concentration N_A^-.

When temperature decreases below 100 K, thermal energy of carriers (holes or electrons) reduces, leading to ionised impurities behaving like shallow traps, then carriers begin to occupy these shallow levels [25]. As the temperature decreases further (<10 K), carriers in semiconductor are fully frozen out. The substrate behaves like an insulator since the thermal energy kT is not sufficient to excite carriers out of their dopant sites [26]. Figure 2.2 shows the changing of ionised acceptor concentration (N_A^-) over a wide range of temperature. If voltage applied on the gate of the transistor is sufficient to excite the carriers into the conduction band, a carrier

channel is formed. For example, consider an NMOS at very low temperatures, when a positive gate bias is applied, no depletion region forms in the substrate under the gate. However, the source/drain wells are degenerately doped and are not frozen out for any temperatures. The applied positive gate bias pulls electrons out of the source/drain wells, forming a sheet of negative charge under the gate. In this manner, an inversion layer has formed without any contributions from the bulk substrate [25, 27].

The ionisation process of the dopant at low temperatures has been discussed in many publications [12, 25, 28]. Three possible types of field dependent ionisation mechanisms are widely reported in literature depending on temperature and applied electric field.

The first mechanism is the Poole-Frenkel ionisation - field assisted thermal ionisation, which is known as the main mechanism forming the channel at temperature from 10 K to 30 K [25]. At this temperature, the trapped carriers in the shallow level do not have enough energy to escape from the barrier. If an application of a field lowers the barrier to thermal ionisation by $\Delta E = q(qF/\pi\varepsilon_{Si})^{1/2}$, the carriers now can be thermally excited over the barrier [28].

The second possible mechanism of field dependent ionisation is by tunnelling. This mechanism is reported as a weakly temperature-dependent process or filed-induced ionisation since the carriers under a strength applied field is able to tunnel through the barrier into the band. However, the tunnelling process is very sensitively to the electric field.

The third mechanism is the shallow-level impact ionisation. When majority carriers are generated by avalanche multiplication for sufficient field near the drain, these carriers flow through the substrate and can induce the ionisation of dopant impurities by impact ionisation. This kind of ionisation seems to be dominant at very low temperature ($< 10K$) for intermediate electric field [12, 28].

The ionisation of the dopant at low temperatures has a significant effect on the device's properties, leading to abnormal behaviour.

2.1.1.2 Incomplete ionisation model

Using Fermi-Dirac statistics with appropriate degeneracy factors for conduction and valence bands, the ionised impurity concentration of donor (N_D^+) and acceptor (N_A^-) are modelled as a function of temperature as [14]

$$N_D^+ = \frac{N_D}{1 + 2e^{\frac{E_F - E_D}{kT}}} \tag{2.1}$$

$$N_A^- = \frac{N_A}{1 + 4e^{\frac{E_A - E_F}{kT}}} \tag{2.2}$$

where E_D and E_A are the ionisation energies of the donor and acceptor impurities, respectively. And E_F is the quasi-Fermi level corresponding to electron or hole concentrations in the doped semiconductor.

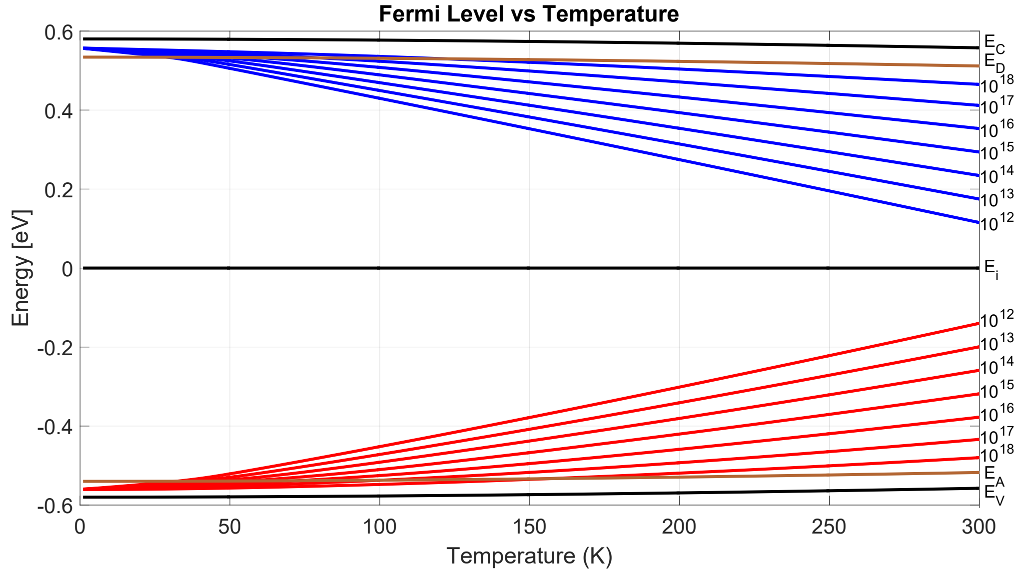


Figure 2.3: Energy diagram: Fermi energy in p-substrate (red line) and n-well (blue line).

Taking into account the impact of temperature on ionised dopant concentration degradation, the Fermi energy in a p-substrate corresponding to acceptor concentrations (N_A) can be determined from [9]

$$E_F = \frac{E_A + E_V}{2} - \frac{kT}{2} ln\left(\frac{N_A}{4N_V}\right) - kT sinh^{-1}\left(\sqrt{\frac{N_V}{16N_A}} e^{-(E_A - E_V)/2kT}\right). \tag{2.3}$$

For an n-well (with donors N_D) in bulk CMOS, the Fermi level can be calculated from

$$E_F = \frac{E_D + E_C}{2} - \frac{kT}{2} ln\left(\frac{N_D}{2N_C}\right) - kT sinh^{-1}\left(\sqrt{\frac{N_C}{8N_D}} e^{-(E_C - E_D)/2kT}\right). \tag{2.4}$$

In both Eq. (2.3) and Eq. (2.3), the Fermi energy is referenced to the intrinsic energy E_i. Figure 2.3 plots the Fermi energy corresponding to variations of dopant concentrations (10^{12} to 10^{18}) over a wide range of temperature. Noting that all parameters, i.e. E_A, E_V, E_D, E_C, can be found in [14].

2.1.2 MOS operation

Basically, with a sufficient voltage applied on the gate terminal, carriers in the channel form an inversion layer (carrier channel) underneath the gate-oxide. If a voltage is applied between source and drain terminal, a current will flow from the drain to the source of the transistor. Following the conventional description of MOS operations, we will present the operation of n-channel MOS (NMOS) in this section unless otherwise mentioned. For p-channel MOS (PMOS), it can be derived from NMOS transistor by inverting the polarity of the biases.

Operations and current-voltage (I-V) characteristics of NMOS transistor is depicted in Fig 2.4. In general, based on the threshold voltage V_T (section 2.2.1 and Chapter 4) and the drain-source voltage V_{DS}, the operation of MOS device can be divided into three regions:

1. Subthreshold region (cutoff region) when $V_{GS} < V_T$
2. Linear region (triode region) when $V_{GS} \geq V_T$ and $V_{DS} < V_{DS,sat}$
3. Saturation region when $V_{GS} > V_T$ and $V_{DS} \geq V_{DS,sat}$

2.1.2.1 The subthreshold regime

When the applied gate voltage is smaller than the threshold voltage ($V_{GS} < V_T$), a weak inversion under the gate from source to drain is formed, the transistor operates in the subthreshold region. The operation of MOS transistor in the subthreshold region is especially important for deep submicrometer devices and for low-voltage operation.

In this region, the drain current I_D is dominated by diffusion which is mainly caused by the gradient of charge from the drain to the source. The drain current can be expressed using following semi-empirical model [29]

$$I_D = I_0 \left(1 - e^{\frac{-V_{DS}}{kT/q}}\right) e^{\frac{V_{GS}-V_T-V'_{off}}{n_0 kT/q}} \tag{2.5}$$

where

$$I_0 = \mu \frac{W}{L} \sqrt{\frac{q\varepsilon_{Si} NDEP}{2\Phi_0}} v_t^2 \tag{2.6}$$

$NDEP$ is the doping concentration, μ is the effective mobility, and n_0 is a fitting parameter describes the subthreshold swing. V'_{off} is the offset voltage that determine the current at V_{GS} = 0 and Φ_0 is the surface potential.

Another subthreshold current model is presented in [30],

$$I_D = \mu C_{ox} \frac{W}{L} (m_0 - 1) \left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_T)}{m_0 kT}} \left(1 - e^{\frac{qV_{DS}}{kT}}\right), \tag{2.7}$$

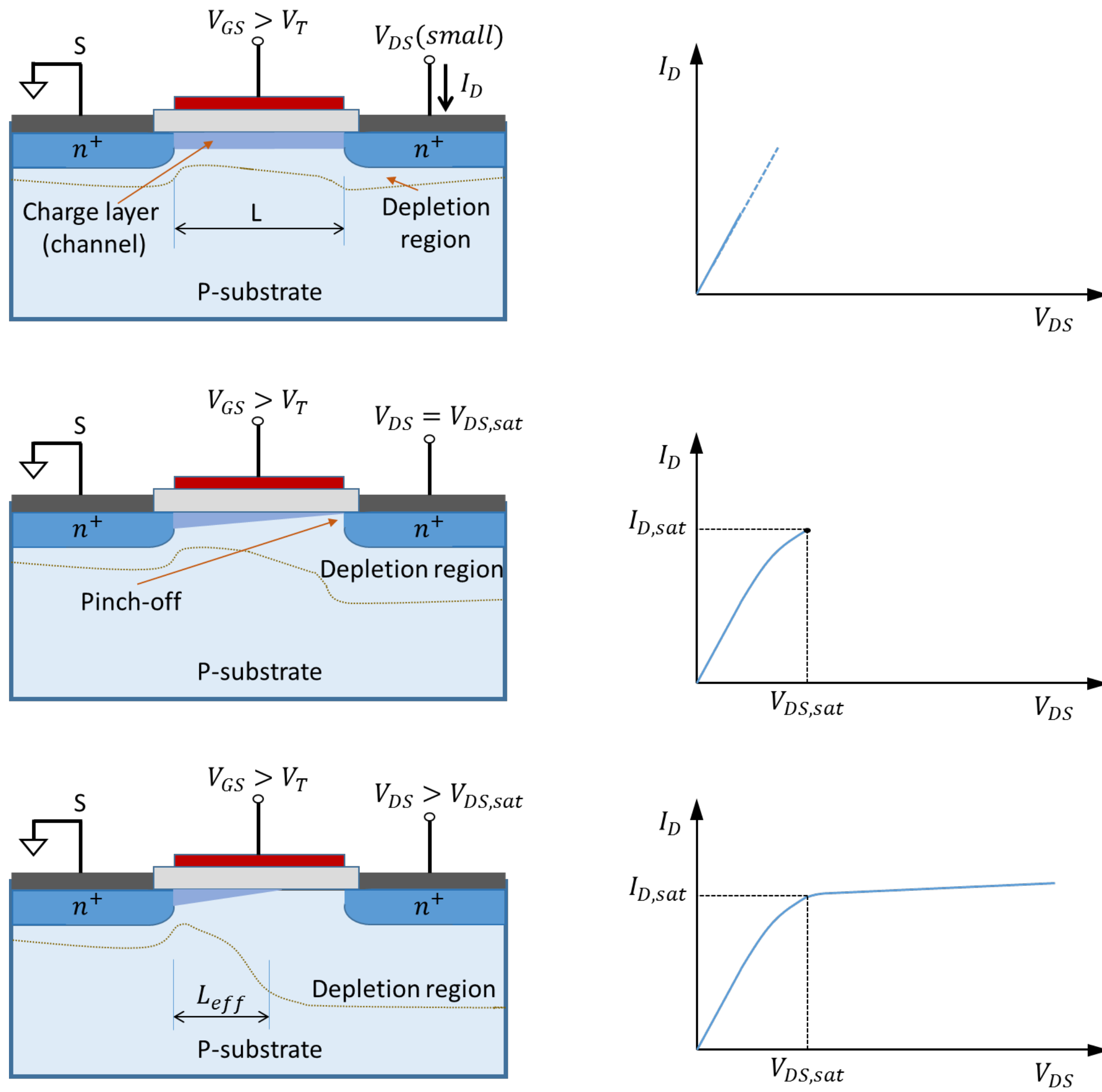


Figure 2.4: Operations and I-V characteristics of NMOS (adapted from [14])

where C_{ox} is the gate-oxide capacitance, and V_{SB} is the source-to-bulk voltage. In Eq. (2.7), m_0 is a fitting parameter. For V_{DS} greater than a few kT, Eq. (2.7) can be rewritten as [31]

$$I_D = \mu C_{ox}\frac{W}{L}(m_0 - 1)\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{GS}-V_T)}{m_0 kT}}. \tag{2.8}$$

Both models can be able to fit experimental data by adjusting the fitting parameters as functions of temperature. However, the accuracy of these models degrades when the subthreshold current is modelled at low temperatures (below 150 K) [9].

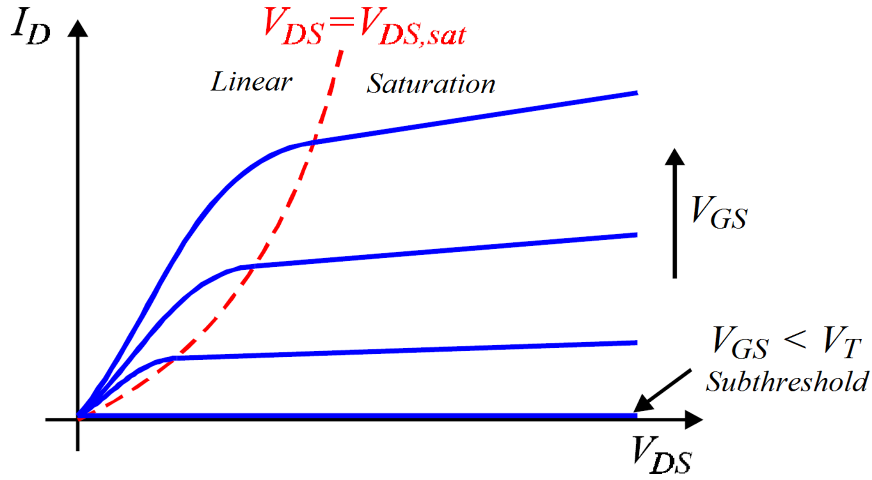


Figure 2.5: MOS operation regions

2.1.2.2 The linear regime

In this region, the drain current is first linearly proportional to the drain voltage, then gradually roll off when V_G approaching a saturation point (V_{DSAT}). The current-voltage characteristic can be expressed by

$$\begin{aligned} I_D &= \frac{W}{L}\mu C_{ox}(V_{GS} - V_T)V_{DS} && \text{when } V_{DS} \ll V_{DSAT}, \\ I_D &= \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_T - \frac{\alpha}{2}V_{DS}\right)V_{DS} && \text{when } V_{DS} < V_{DSAT}. \end{aligned} \tag{2.9}$$

The "smoothing" parameter α in Eq. (2.9) corresponds to a relation between the depletion region depth at the source and along the channel [24]. It can be calculated from

$$\alpha = 1 + \frac{\gamma}{2\sqrt{\Phi_0}}, \tag{2.10}$$

where γ is the body effect, and Φ_0 is the surface potential. At room temperature, $\alpha = 1$ is normally used in a hand calculation (SPICE level 1). However, for better results, α can be varied depending on technologies from 1 to 1.3. At low temperatures, α can be used as a fitting parameter in a simple model (i.e. SPICE level 3) to obtain a good I-V description.

The saturation voltage V_{DSAT}, a drain voltage at which the inversion layer charge at the drain side is zero, is determined as follows

$$V_{DSAT} = \frac{V_{GS} - V_T}{\alpha}. \tag{2.11}$$

It is worth noting that V_{DSAT} value changes when temperature decreases since both α and threshold voltage V_T change.

2.1.2.3 The saturation regime

When the gate voltage is greater than the threshold voltage, and the drain voltage is higher than the saturation voltage, the transistor operates in the saturation regime. In this region, the I_D is mainly dominated by drift current, which is proportional to the electric field from the drain to the source. The drain current can be considered as a constant regardless of an increase in the drain voltage.

The conventional formula of the saturated current, used for analysis and hand calculation, is

$$I_D = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_T - \frac{\alpha}{2}V_{DSAT}\right)V_{DSAT}. \tag{2.12}$$

This model is normally used to model a long channel transistor and ignores several effects such as channel length modulation and the short channel effect [24].

2.1.3 MOS models

In previous sections, I-V models for transistors operating in all regions were introduced. These simple models, known as SPICE level 1, took an implicitly physical approach to describe transistor characteristics. They are conventionally used for long channel device analysis and hand calculations. For sub-micrometer technologies, I-V models need to employ “smoothing functions” to model effects of device geometries [32]. For example, the MOS3 model is the level 3 model from Berkeley SPICE and is a semi-empirical model which incorporates most of the second-order small-size effects. The drain current in MOS3 model is expressed as [33]:

For the linear region:

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GST} - \frac{(1+F_B)}{2}V_{DS}\right)V_{DS}\frac{1}{1+T0}\ , \tag{2.13}$$

For the saturation region:

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GST} - \frac{(1+F_B)}{2}V_{DSAT}\right)V_{DSAT}\frac{1}{1+T0}\ , \tag{2.14}$$

where C_{ox}, W, L have their conventional meanings, and μ is the effective mobility, while V_{GST} = V_{GS} - V_T, with V_T is the threshold voltage. F_B is a coefficient accounting for short-narrow channel effects and is calculated by

$$\begin{aligned}
F_B &= \frac{\gamma F_S}{4\sqrt{2\phi_F - V_{BS}}} + F_N \\
F_N &= \frac{\delta_W \pi \varepsilon_{Si}}{2C_{ox}W} \\
F_S &= 1 - \frac{xj}{L}\left[\left(\frac{ld}{xj} + \frac{W_C}{xj}\right)\sqrt{1-\left(\frac{W_p}{1+W_p}\right)^2} - \frac{ld}{xj}\right] \\
W_p &= \frac{X_D}{xj}\sqrt{2\phi_F - V_{BS}} \\
X_D &= \sqrt{\frac{2\varepsilon_{Si}}{qN_{sub}}} \\
\frac{W_c}{xj} &= 0.0631353 + 0.8013292W_p - 0.01110777{W_p}^2.
\end{aligned} \tag{2.15}$$

Detailed values and meaning of parameters in Eq. (2.15) are provided in [33]. The saturation Drain-Source voltage V_{DSAT} and the current saturation factor T_0 are determined by

$$V_{DSAT} = V_{GST} + E_C L - \sqrt{{V_{GST}}^2 + E_C L^2}, \tag{2.16}$$

$$T_0 = \frac{\mu V_{DSAT}}{V_{sat} L}, \tag{2.17}$$

where V_{sat} is the maximum velocity, and $E_C = \frac{V_{sat}}{\mu}$.

For circuit simulation, models from BSIM Group are widely used in most of the commercial simulation tools [23]. BSIM models, i.e. BSIM4, are derived from physics and fitting parameters that allow it to model all effects of both long and short channel devices (28 nm) at room temperature [29, 34]. Other advantage MOSFET models, such as EKV (Enz-Krummenacher-Vittoz) [35], PSP (the name is not an acronym) [36] or HiSIM model (Hiroshima University Semiconductor Technology Academic Research Center IGFET Model) [37], have become more

popular in circuit simulations for deep submicrometer transistors. Nevertheless, none of these models can be used for low-temperature circuit simulations.

2.2 MOSFET parameters

Studies on bulk MOSFET parameters at cryogenic temperatures have been reported [9, 10, 38–44]. A proper understanding of MOSFET parameter variations caused by decreasing temperature will reveal the MOS characteristics at the examined temperatures. Most semiconductor parameters vary as temperature changes but some show only a relatively small dependence, while others may change by several orders of magnitude. The following section reviews some common MOSFET parameters and how their properties change as temperature decreases.

2.2.1 Threshold voltage

Threshold voltage is one of the fundamental parameters of the MOS transistor which is considered as an indicated factor in transistor analysis as well as in reliability evaluation. Threshold voltage is defined as the point when the substrate immediately underneath the gate oxide starts to be inverted, forming a carrier channel between the source and drain [14]. In practice, the threshold voltage can be determined experimentally based on charge-based methods, which defines the threshold voltage as the voltage where the diffusion current is equal to the drift current in the substrate [45]. In this work, however, the classical surface potential-based threshold voltage model - the most popular model in commercial circuit simulations, i.e. BSIM models, is used to develop a model for cryogenic temperature simulations. In a long N-channel device at zero substrate bias, the threshold voltage is given as [24]

$$V_{T0} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0}\ , \tag{2.18}$$

where V_{FB} is the flat-band voltage, γ is the body-effect coefficient, and ϕ_0 is the surface potential. Also, $V_{FB} = -|\phi_F| - \phi_{gate} - \frac{Q'_0}{C'_{ox}}$, where $|\phi_F|$ is the Fermi potential, ϕ_{gate} is the work function of the gate, Q'_0 represents the effective oxide charge per unit area, and C'_{ox} is the gate capacitance per unit area. In strong inversion, $\phi_0 \approx 2|\phi_F|$, thus Eq. (2.18) becomes

$$V_{T0} = |\phi_F| - \phi_{gate} - \frac{Q'_0}{C'_{ox}} + \gamma\sqrt{2|\phi_F|}\ . \tag{2.19}$$

It is well known that the threshold voltage changes as devices are scaled. This is due to several phenomena such as non-uniform of doping concentrations, charge sharing effects and the Drain Induced Barrier Lowering (DIBL) effect [24]. At room temperature, effects of device

geometries on the threshold voltage, effectively modelled in the BSIM model, are given by [46]

$$V_T = V_{T0} + \Delta V_T \ , \tag{2.20}$$

and,

$$\Delta V_T = \Delta V_{Vdop} + \Delta V_{Ldop} + \Delta V_W - \Delta V_{WL} - \Delta V_L - \Delta V_{DIBL}. \tag{2.21}$$

Here, ΔV_{Vdop}, ΔV_{Ldop} are the non-uniform doping of the substrate in vertical and horizontal (lateral) axis, ΔV_{DIBL} is the DIBL effect, while ΔV_W, ΔV_L, ΔV_{WL} are the narrow channel effect, the short channel effect, and the short and narrow effect, respectively. Detailed expressions of these effects are provided in Appendix B.

In Eq. (2.19), ϕ_{gate} has almost no temperature dependence due to the gate being degenerately doped [9], and $\frac{Q'_0}{C'_{ox}}$ can be assumed constant in strong inversion [47]. When temperature decreases, the magnitude of Fermi potential, Φ_F, increases due to a decrease of ionised dopant concentration, and hence, the threshold voltage increases. A monotonic increase of threshold voltage with the reduction of temperature can be observed for both PMOS and NMOS.

A number of studies have measured from various processes and reported the shifting of the threshold voltage at room and cold temperatures. For example, a study of Gaensslen et al. investigated the characteristics of n-channel MOSFETs with channel lengths of the order of 1 μm in the temperature range from 300K down to 77.3 K. It showed that threshold voltage of the transistor increases when cooling down to liquid nitrogen temperature [48]. In [49], authors investigated the operation of bulk CMOS devices working at liquid nitrogen temperature (77 K) by examining both Silicon-On-Insulator (SOI) and bulk MOSFET devices. Measured results showed that both devices exhibit an increase in the threshold voltage when the devices are cooled. They concluded that the shift in the bulk MOSFET threshold voltage was higher than that in SOI transistors. A characterisation study on 2 μm bulk CMOS at liquid helium temperature (4.2 K) had confirmed the threshold voltage of both PMOS and NMOS continued to increase when the temperature reached 4.2 K [50]. Measured results showed that the shifting threshold voltage of 2 μm NMOS is 0.59 V from room temperature to 1.08 V at 4.2 K. And in the same manner, threshold voltage of PMOS increases from -0.74 V to -1.43 V. In another work, properties of smaller CMOS transistors (1.3 μm high performance CMOS or Hi-CMOS process) at deep cryogenic temperature was presented in [51]. It also reported that the shifting of the threshold voltage of NMOS from 300 K to 4.2 K is 0.45 V, whereas that of PMOS is -0.39 V.

Table 2.1: The changing of threshold voltage (V) of different Bulk CMOS processes at room and cold temperatures

Process	300K	77K	4.2K	Size (L,W,T_{ox})	Ref.
2μm Hi-CMOS (N-PMOS)	0.59 -0.74	1.04 (76.3%) -1.20 (62.2%)	1.08 (83.1%) -1.43 (93.2%)	L=2μm W=- T_{ox} = 35nm	[50]
1.3μm CMOS (N-PMOS)	0.31 -0.49	0.68 (119.4%) -0.85 (73.5%)	0.76 (145.2%) -0.88 (79.6%)	L=1.3μm W=15μm T_{ox} = 20nm	[51]
0.7μm CMOS (N-PMOS)	0.76 -0.97	-	1.05(38.2%) -1.05 (8.2%)	L=0.7μ W=70μ T_{ox} = 15nm	[52]
0.35μm CMOS (PMOS)	-0.95	-1.40 (47.4%)	-	L=10μm W=100μm T_{ox} = 7.6nm	[53]
0.35μm CMOS (NMOS)	0.55	-	0.89 (61.8%)	L=0.35μm W=4.45μm T_{ox} = 7.6nm	[47]
0.35μm CMOS (N-PMOS)	0.51 -0.65	0.68 (33.3%) -1.16 (78.5%)	-	L=2μm W=10μm	[16]
0.25μm CMOS (N-PMOS)	0.46 -0.51	-	0.62 (34.8%) -0.84 (64.7%)	L=0.25μ W= - T_{ox} = 7nm	[54]

A summary of threshold voltages of bulk CMOS at low temperatures is presented in Table 2.1. It is clear to see that the increase in threshold voltage V_T for PMOS and NMOS is asymmetric. In most cases, the shifting rate of V_T looks quickly when temperature reduces from room to about 77 K then gradually increases.

2.2.2 Mobility

Mobility of carriers (holes and electrons) is another fundamental parameter of MOS transistor. Studies of this parameter reveal carrier transport in the device channel and help to understand device characteristics. Several works have investigated carrier mobility, providing both theory and practical models for carrier mobility from room temperatures (300 K) down to liquid helium temperature 4.2 K) [42, 43, 55–59].

In general, mobility of carriers, μ, can be expressed as an inverse function form which is a sum of scattering rates corresponding to all relevant scattering modes (Mathiessen rule) [14, 28, 60]. This is expressed by

$$\frac{1}{\mu} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{cs}} + \frac{1}{\mu_{sr}}, \tag{2.22}$$

where μ_{ph} represents for the phonon scattering caused by the lattice vibrations, μ_{cs} is called Coulomb scattering which is related to the electrically charged ionised impurity atoms. The scattering due to surface roughness, μ_{sr}, which accounts for the effect of the surface on the mobility of electrons near the semiconductor oxide interface.

At a given temperature, carrier mobility is studied as a function of (average) electric field. While Coulomb scattering is the main source limiting the carrier mobility at low fields, increasing the field leads to the inversion layer charge, and phonon scattering becomes dominant. As the field increases further, the accumulation of charges towards the Si/SiO_2 surface cause the surface roughness to become the major scattering mechanism, resulting in mobility degradation.

These scattering mechanisms also vary as temperature changes. Since the phonon scattering results from thermal vibration, at room temperature, the carrier mobility is mainly derived from phonon scattering. As temperature increases, the lattice vibrations increase; hence the mobility decreases. When temperature reduces, the Coulomb and the surface roughness processes prevail resulting carrier mobility varies as temperature changes.

To quantify the mobility, each scattering element is separately evaluated. For phonon scattering, μ_{ph} varies with the effective electric field and is written as

$$\mu_{ph} = AE_{eff}^{\gamma} T^{\alpha_{ph}}. \tag{2.23}$$

Here A and γ are constant coefficients, while α_{ph} is a power factor of temperature T. Noting that, these parameters are different for electrons mobility and holes mobility [60, 61].

For surface roughness scattering, μ_{sr} is mainly dependant on the effective electric field, and can be empirically represented as [60, 61]

$$\mu_{sr} = BE_{eff}^{-\beta_{sr}}, \tag{2.24}$$

where E_{eff} is the effective electric field, B and β_{sr} are fitting parameters.

For Coulomb scattering, μ_{cs} is inversely proportional to the charge density and has linear variation with energy [14, 60]

$$\begin{aligned} \tau_c &= cN_{sub}^{n_c}, \\ \mu_{cs} &= \frac{\tau_c q}{m^*}, \end{aligned} \tag{2.25}$$

where τ_c is the mean free time between collisions due to Coulomb scattering with fitting parameter c, n_c. And, N_{sub} is the ionised concentration in the substrate while m^* is the effective mass of electrons or holes.

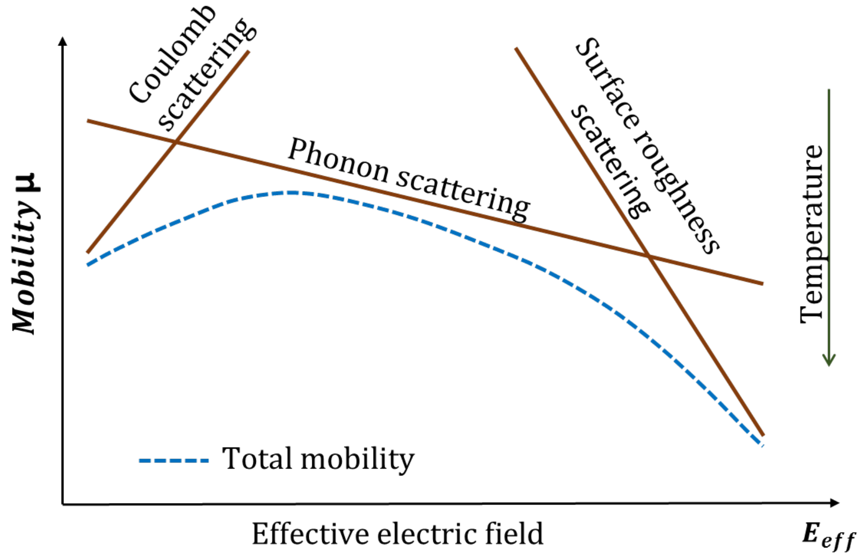


Figure 2.6: Dominant scattering mechanisms in carrier mobility (adapted from [60].

Although it can be distinguished from physical factors dominating on the carrier mobility at a given temperature, it is difficult and complicated to formulate the mobility based on the physics. Semi-empirical models, derived from physics and fitting parameter, are normally used for modelling the carrier mobility. One of the common formulas of effective mobility in channel of MOSFET device is given as [24]

$$\mu_{eff} = \frac{\mu_0}{1-(a_\theta/\varepsilon_{Si})(Q_B+\eta_E Q_I)}, \tag{2.26}$$

where μ_0 is low field mobility, a_θ is a fitting parameter, and ε_{Si} is the dielectric constant of silicon. Both μ_0 and a_θ are temperature dependence. For lightly doped substrates, μ_0 varies in a range 350 - 600 cm^2/Vs for electrons and 100 - 200 cm^2/Vs for holes, while a_θ has a value around 10^{-6} at room temperature [24].

In Eq. (2.26), Q_B and Q_I are the depletion region and inversion layer charges, respectively. Since it is complicated to determine Q_B and Q_I in the channel, average values between source and drain terminals are used to approximate these charges [62].

A semi-empirical mobility model for 50–300 K temperature range was proposed in [58] which employed fitting parameters to model the change in mobility when temperature decreases. Another semi-empirical model based on inversion charge, Q_i, is introduced in [57]. This model

fits low field mobility in a long channel device over a wide range of temperature, given as

$$\frac{1}{\mu} = \frac{A}{Q_i^{n-2}} + BQ_i, \tag{2.27}$$

where n is an exponent coefficient which varies from 2 to 3 as temperature reduced from room to liquid helium temperature. In Eq. (2.27), A and B are constants depending on the strength of the Coulomb and surface roughness scattering rates which are determined as

$$\begin{aligned} A &= \frac{C_{ox}^{n-2}}{\theta^{n-2}\mu_g}, \\ B &= \frac{\theta}{\mu_g C_{ox}}, \end{aligned} \tag{2.28}$$

where θ is the mobility attenuation factor, μ_g is generalised mobility parameter related to the maximum effective mobility as $\mu_g = \mu_0$ for $n = 2$ and $\mu_g = (n-1)(n-2)^{(n-2)/(1-n)\mu_m}$ for $2 < n \leq 3$.

In the relation versus the gate voltage V_{GS}, the effective mobility can be written as [10]

$$\mu = \mu_m \frac{[\theta(V_{GS} - V_T)]^{n-2}}{1 + [\theta(V_{GS} - V_T)]^{n-1}}, \tag{2.29}$$

where μ_m is proportional to the maximum mobility, and V_T is the threshold voltage.

For sub-micrometer technologies, an increase in the electric field due to a reduction of gate oxide thickness resulting a change in scattering mechanism [63, 64]. Consequently, a second attenuation factor θ_2 is introduced to model this effect, and Eq. (2.29) is rewritten as [41]

$$\mu = \mu_m \frac{[\theta(V_{GS} - V_T)]^{n-2}}{1 + [\theta(V_{GS} - V_T)]^{n-1} + [\theta_2(V_{GS} - V_T)]^{n}}. \tag{2.30}$$

The increase of mobility magnitude at low temperatures has been reported in several works. For example, measurements in [65] showed that mobility increases by a factor of 4-6 when temperature is decreased from 300 K to 77 K. This investigation using 0.5 μm CMOS technolog revealed that both mobility of electrons in NMOS, and holes in PMOS, depend on temperature by the factor of $T^{-1.3}$ and $T^{-1.2}$, respectively. The authors also confirmed that the increase transconductance of long channel transistor is higher than that of the short channel. The increase of mobility of CMOS devices was also confirmed at deep cryogenic temperatures (i. e.l 4.2 K) in the study of Aoki et. al which investigated the sub-micrometer Hi-CMOS III technology. It is reported that the improvement of mobility of n-channel is greater than p-channel MOS and less significant in thinner oxide devices at a V_{GS} of nearly 5V [51]. The work in [66] also confirmed that the mobility - in 90 nm n-channel MOS at 4.2 K, improved by a factor of 5.6 compared to

that at room temperature. A summary of mobility increase with decreasing of temperature is shown in Table 2.2.

Table 2.2: The increase of carrier mobility of Bulk CMOS processes at cold temperatures versus room temperature (@ E_{eff} = 0.1 MV/cm)

$\frac{\mu}{\mu_{300K}}$	77 K	4.2 K	Note	Ref.
NMOS PMOS	6 4	-	0.5 μm CMOS	[65]
NMOS PMOS	6 6	-	$N_A = 3.9x10^{15}$ $N_D = 1.6x10^{16}$	[60]
NMOS	4	15	W/L = 25/25 [um] t_{ox} = 28 nm	[28, 43, 67]
NMOS PMOS	3 4	3.5 2.5	Hi-CMOS L= 2mum	[50, 51]
NMOS	4.7	-	0.35 mum CMOS W/L = 10/2 [um]	[16]
NMOS	6	10	0.35 mum CMOS W/L = 1/1 [um]	[68]
NMOS PMOS	6.6 6.3	-	0.35μm CMOS W/L = 10/2 [um]	[16]
NMOS PMOS	-	3.3 2.7	0.25μm CMOS W/L = 10/0.25 [um]	[54]
NMOS PMOS	3.0 2.7	-	0.25μm CMOS $N_A = 3x10^{16}$	[69]
NMOS	-	5.6	W/L = 5/0.09 [um] t_{ox} = 1.5 nm	[66]

2.2.3 Transconductance

In mixed signal and digital applications, transconductance g_m is used to evaluate speed and output drive ability. This parameter is defined as a variation of the drain current that corresponds to a variation of the gate voltage at a fixed source-drain voltage V_{DS}. Using the drain current in Eq. (2.9) and Eq. (2.12), g_m is given as

$$\begin{aligned} g_m &= \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} \\ &= \mu C_{ox}\frac{W}{L}V_{DS} && \text{in linear region;} \\ &= \mu C_{ox}\frac{W}{L}(V_G - V_T) && \text{in saturation region.} \end{aligned} \tag{2.31}$$

For a long channel, increases of mobility μ with decreasing temperatures makes transconductance g_m increase. For example, g_m of long channel N-MOSFET (W = L = 13 μm) at 77 K is 6 times greater than the value at 300 K, whereas, for short channel (W/L = 10/0.24 μm), it increases by approximately 2.7 times [17]. In another work, the transconductance of 90 nm NMOS (W=16x5 μm) at 4.2 K was 1.5 times higher than that at 300 K [66]. Also, the transconductance increased almost linearly with the decrease of temperature from 300 K down to 25 K before slightly decreasing at temperatures below 25 K due higher series resistance in the lightly doped source/drain regions (LDDs) [66].

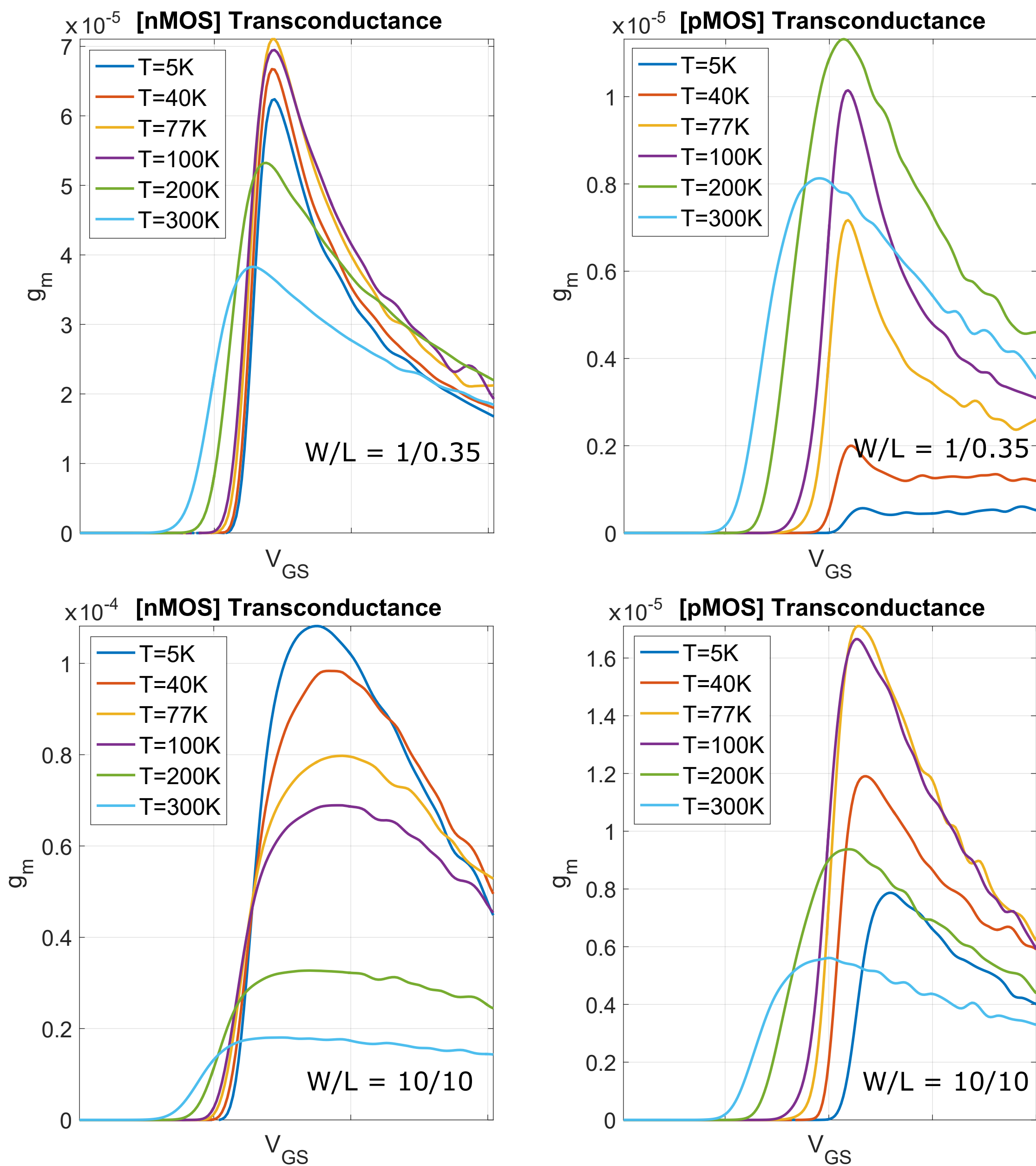


Figure 2.7: Measured transconductance at different temperatures.

The increase in transconductance of long channel transistors was higher than that of short channel transistors as shown in [51, 65]. To verify the increase of the transconductance with decreasing temperatures, in this work, I_D-V_{GS} characteristics of bulk 0.35 μm CMOS were measured from the room temperature down to liquid helium temperature. The details circuits and experimental setup will be presented exclusively in section 6.2, Chapter 6. Experimental results as shown in Fig. 2.7, g_m exhibits the same results in long channel PMOS and NMOS. In particular, g_m in NMOS devices increased with decreasing temperature while that in PMOS transistors reached a peak value of 77 K then gradually decreasing when temperature further decreases. However, in short channel devices, especially in PMOS, transconductance decreased at very low temperatures. The reason for this phenomena is due to the impact of freeze-out carriers in short channel leading to the increase in threshold voltage and mobility degradation. Another reason could be due to the effect of series resistance and the drain threshold voltage V_{Td} at cold temperatures [70]. The effect of V_{Td} will be discussed in section 2.3.4.

2.2.4 Subthreshold Slope

Subthreshold slope 1/S (or subthreshold swing) is an important parameter in indicating turn-off capability of MOS transistor. In the other words, this parameter is used to evaluate leakage current when transistors are inactive. At a given temperature, its value per decade is given as [24]

$$S = \frac{\partial V_{GS}}{\partial log I_D} = \frac{2.3kTn}{q}, \tag{2.32}$$

where k is Boltzmann's constant, T is absolute temperature, q is electric charge, and n is average body effect coefficient. The quantitive n can be approximated from [24]

$$n = 1 + \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}, \tag{2.33}$$

where Φ_F is Fermi potential, and γ is the body effect coefficient.

As seen from Eq. (2.32), the subthreshold slope is linearly proportional to the temperature such that S reduces as the MOS transistor cools down. This advantage property confirms that MOS devices operating in cold environment are able to achieve a higher performance in terms of speed and power dissipation. A study [65] has reported an increase in the subthreshold slope by a factor of 4 when measuring n-MOSFETs at 77 K. This parameter of 0.25 μm p-MOSFETs measured at 82 K is 30 mV/dec, which is 2.7 times more effective than at 300 K [71]. Measured results of the slope S from both p- and n-channel transistors are similar as shown in [51, 72]. At 43 K, the slope 1/S of 0.35 μm Bi-CMOS is approximately 4 times greater, relative to its 300

K value [72]. And at 4.2 K, the subthreshold characteristic of 0.13 μm NMOS is 10 mV/dec, compared to 80 mv/dec at room temperature [51].

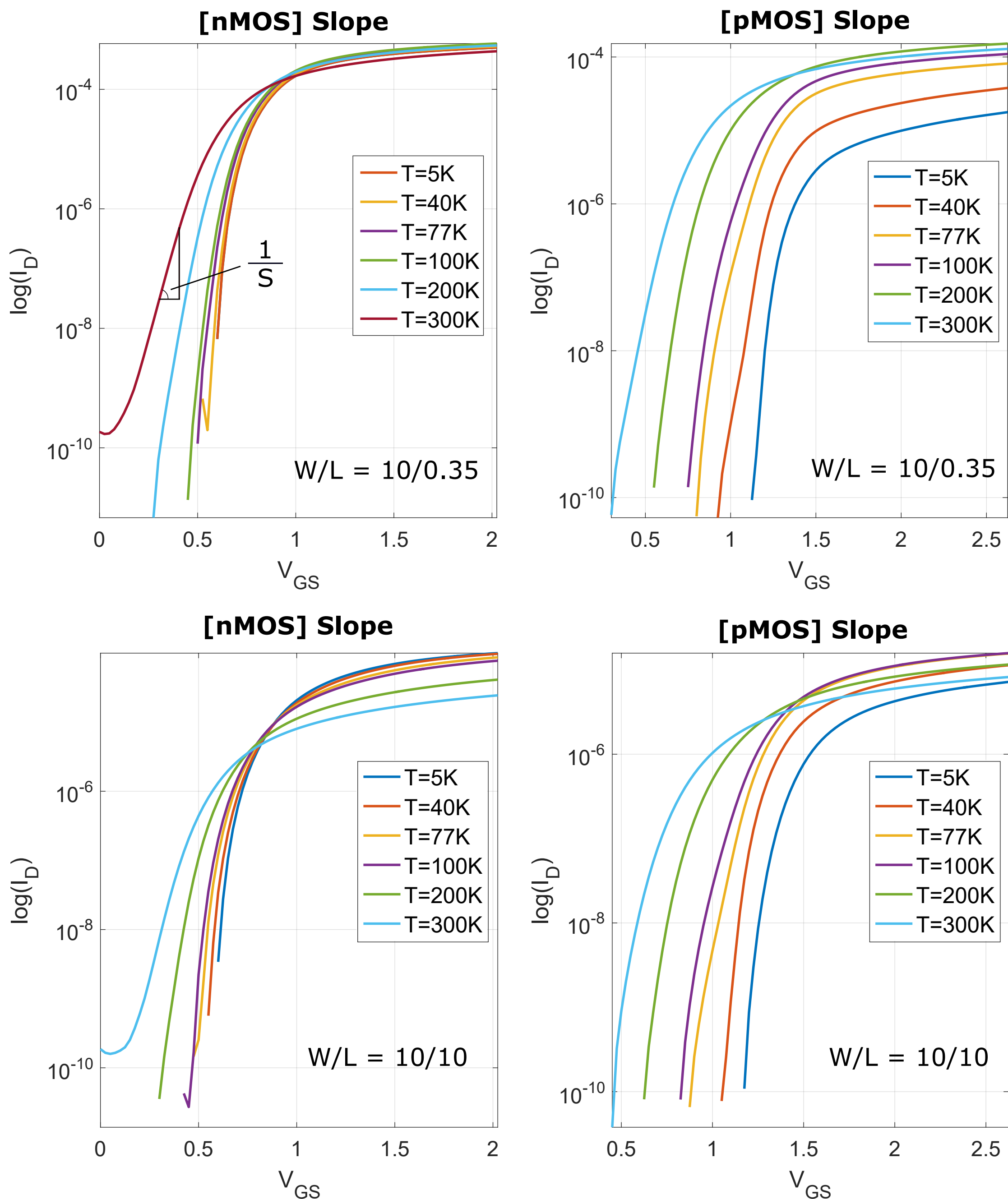


Figure 2.8: Measured subthreshold slope at different temperatures.

In our study, variations of the subthreshold slope, of PMOS and NMOS from room temperature down to 5 K, are shown in Fig 2.8 and summarised in Table 2.3. The turn-off characteristic of n-type devices steadily improves in both long and short channel, whereas, those of p-type

devices presents inconsistent enhanced as temperature decreases. More specifically, the slopes of NMOS and PMOS are about 8 and 1.5 times greater at 5 K compared to those at 300 K, respectively.

Table 2.3: Variations of measured subthreshold slope 1/S

S mV/dec	5 K	40 K	77 K	100 K	200 K	300 K
W/L = 10/0.35						
NMOS	10.3	20.3	20.0	32.9	44.0	81.6
PMOS	35.0	44.6	31.4	45.8	52.3	68.1
W/L = 10/10						
NMOS	13.5	23.5	28.8	37.8	49.2	84.0
PMOS	28.1	38.8	42.1	56.5	60.3	56.4

2.2.5 Gate-oxide capacitance and junction capacitance

Capacitance is one of the main parameters to decide the speed and operating frequency of CMOS circuits. The main capacitance in MOS transistor is gate-oxide capacitance, C_{ox}, defined as [24]

$$C_{ox} = \frac{k_{ox}\varepsilon_0}{T_{ox}}, \tag{2.34}$$

where T_{ox} is the thickness of the oxide, k_{ox} is the dielectric constant of the insulator, i.e. for SiO_2, k_{ox} = 3.9; and ε_0 is the permittivity of free space.

It is reported that the gate-oxide capacitance is almost temperature independent when the MOS transistor operates in the inversion region ($V_{GS} > V_T$) [39, 47, 65]. However, in the accumulation region or depletion region, C_{ox} decreases significantly with falling temperature (see Fig 2.9) due to carrier freeze-out effects, which means all extra carriers (electrons/holes) are captured by their dopant [47].

A study of parasitic capacitance of MOS transistor has shown that junction capacitors, which proportional to the depletion layer depth, drop drastically by a factor of ten at liquid helium temperature compared to the value at room temperature because of the freeze-out carriers in the substrate [47]. Another study of 0.25 μm revealed the declines of bottom junction capacitance and source drain junction sidewall capacitance at 4.2 K were about 50% of those values at 300 K [54]. The improvement in parasitic capacitance is one of the factor, that help with enhancing the performance of MOS transistor at low temperatures.

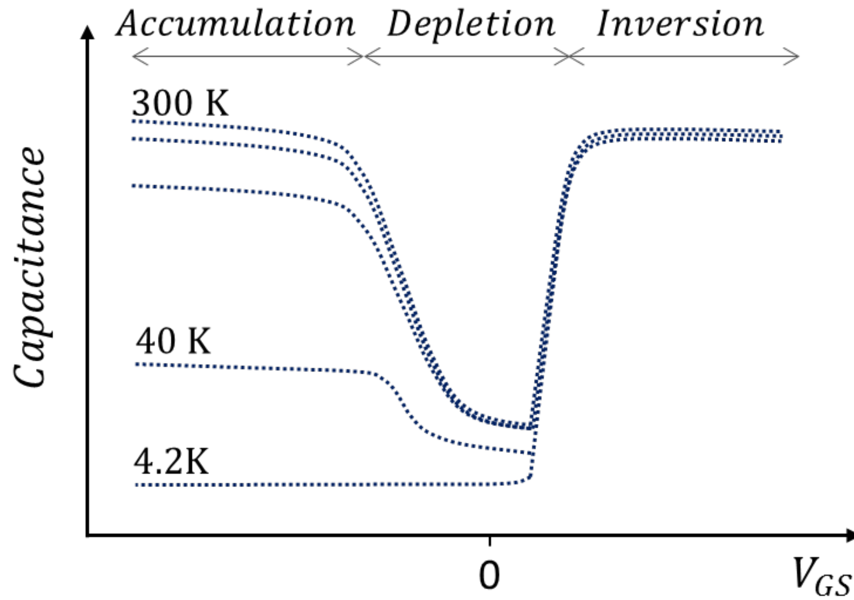


Figure 2.9: Variations of gate-oxide capacitance at different temperature (adapted from [47]).

2.2.6 Channel and parasitic resistance

Channel resistance and source/drain series resistance of a MOS transistor are usually used to explore device reliability. Based on Ohm's law, the total resistance in a channel MOS transistor operating in the strong inversion region is given from

$$R_{tot} = R_{ch} + R_{sd} = \frac{V_{DS}}{I_D}, \tag{2.35}$$

where R_{ch} is the channel resistance, and R_{sd} is the source/drain series resistance including contact resistance R_{ct}, source/drain diffusion resistance R_{diff}, and crowding resistance R_{cr} (the resistance under the gate) [9].

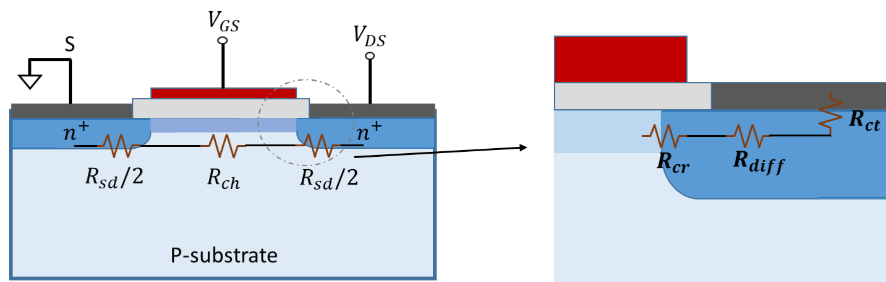


Figure 2.10: Resistance in MOS device.

Since there is an improvement in carrier mobility, the channel resistance decreases with temperature. A comparison between 300 K and 77 K showed that R_{ch} droped from 15 Ω to 12 Ω, taken from 0.18 μm nMOSFET at V_{GS} = 1.0 V and V_{DS} = 1.8 V [39].

In contrast, the value of source/drain series resistance, R_{sd}, much depends on applied extraction methods [73]. In general, the source/drain series resistance of both n-type and p-type devices decrease when the temperature droped down to 77 K. For example, R_{sd} of PMOS and NMOS decrease about 50% and 25%, respectively, as temperature droped between 300 K down to 77 K [65]. In [74], 0.6 μm PMOS had a dropping ratio 2.7 when the transistor was measured at V_{GS} = 2 to 4 V. When temperature further decreases to 4.2 K, due to strong freeze-out effect, R_{sd} becomes greater. Results in [47] showed R_{sd} = 473 Ω at 4.2 K compared with 343 Ω at 300 K. The increase of series resistance of PMOS at 4.2 K is much higher than that of NMOS, 44% versus 5% respectively [54]. In [75], however, R_{sd} was reported increasing at 77 K, whereas, R_{sd} was observed with a steady degradation from room temperature down to 4.2 K [9]. These contradicting results are believed to be caused by problems in extracting the series resistance over a wide range of temperature. In the next chapter (Chapter 3), we will present a new approach for series resistance extraction, applicable from room temperature down to liquid helium temperature.

2.3 Anomalous behaviours

The freeze-out of the carriers at very low temperatures (i.e. $T < 30$ K) lead to some anomalous behaviours in MOSFET operation.

2.3.1 Kink effect

This effect is known as a sharp increase of the drain current in the saturation region with a small changing of the drain-source voltage (Fig. 2.11). The reason of this effect is the self-polarisation of the bulk silicon due to the injection of the excess carriers into the substrate by the impact ionisation at the drain. At very low temperatures, the impact ionisation is observed at a lower V_{DS} due to the increased multiplication factors. The excess carriers injected into the substrate cannot be collected effectively by the substrate contacts, since the resistance of the bulk silicon significantly increases due to the impurity freeze-out. This phenomenon has been reported in several studies [10–12, 26, 76]. However, in many recent works [16, 47, 54], the kink effect is not clearly observed in sub-micrometer devices. The combined effects of charge sharing and velocity saturation with temperature in short channel transistor help relieve this effect [77].

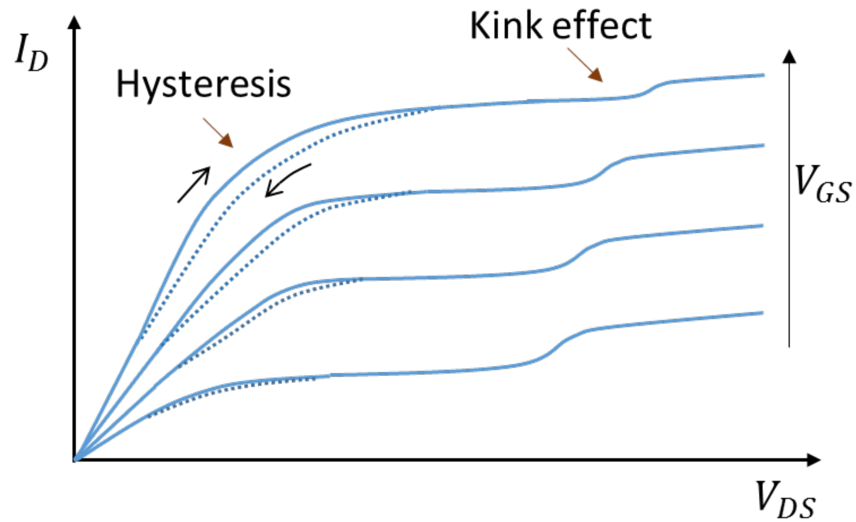


Figure 2.11: Kink and hysteresis effect on I-V characteristic of MOSFET at low temperatures

2.3.2 Hysteresis

As shown in Fig. 2.11, the I_D curves, as a function of V_{DS} are not identical when sweeping V_{DS} from low-to-high and reversed. This phenomenon is caused by the slow recharging of the traps between the gate oxide and the silicon substrate since the ionisation rate is low at low-temperature [12, 13]. During the transition, from the linear to the saturation region, the formation of the depletion layer is delayed, resulting in a further increase in the current until a sufficient amount of V_{DS} is achieved. After this point, the current drops to its stable saturation value, which is equal to the value during the high to low V_{DS} sweep [15,27,78].

2.3.3 Latch-up

The latch-up phenomenon is a critical issue in CMOS technologies. This phenomenon could lead to circuit malfunction, followed by the destruction of the device [24]. In bulk CMOS technologies, the combination of substrate and n-/p-well creates a parasitic n-p-n-p path or parasitic bipolar transistors (Fig. 2.12). Latch-up occurs when both parasitic BJTs conduct creating a low resistance path from Vdd to Gnd, and the product of the current gain of Q1, Q2 in the feedback loop is greater than 1 ($\beta_1\beta_2 > 1$).

At low temperatures, due to the increase of mobility, the substrate and well resistances decrease. If the temperature is decreased further, these resistances do not have ohmic behaviour due to the freeze-out of carriers. Therefore, a barrier must be overcome to achieve conduction.

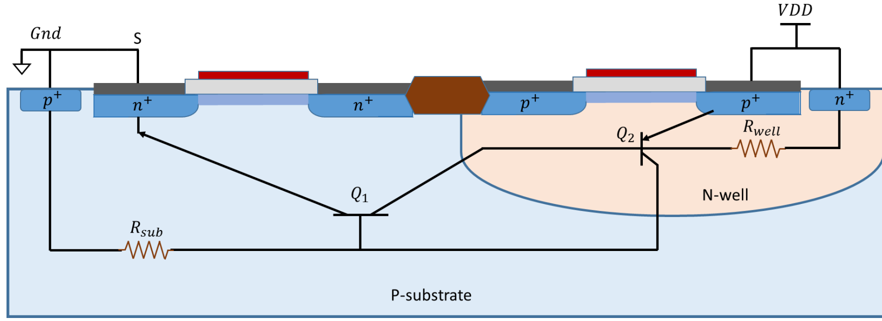


Figure 2.12: Intrinsic bipolar junction transistors in bulk CMOS

Moreover, a decline in gain current factors β of the parasitic transistors could prevent this unwanted phenomenon at temperatures below 50 K [79, 80]. The presence of a high electric field could induce latch-up because the behaviour of parasitic bipolar transistors can differ from that of a diffusion limited bipolar transistor [79].

In practical design, layout techniques, such as ring protection or proper substrate/well contacts, are used to prevent latch-up in CMOS [81]

2.3.4 Impact of LDD structures

To suppress the effect of hot carriers in submicron technologies, lightly doped drain (LDD) regions are implemented. This structure, however, could make source/drain resistance larger, which is undesirable. When the temperature is lowered, the impact of LDD structure on the operation of MOS transistor becomes more noticeable. It is reported that this structure strongly affects the transistor operating in the linear region when the temperature is below 100 K [41]. In such a case, freeze-out carriers in the non-degenerate LDD region leads to a signification increase in the LDD series resistance, resulting in a total deactivation of the transistor.

Figure 2.13 depicts the variation of LDD series resistance as a function of electric field E_{LDD} at cryogenic temperatures. A formula to determine series resistance of LDD region has been proposed in [10], given as

$$\begin{aligned} R_{sd} &= R_0 \frac{N_D}{N_D^+} \\ &= R_0 \left(1 + \frac{N_{D0}^+/N_D - 1}{1+\gamma}\right), \end{aligned} \tag{2.36}$$

where N_D, N_D^+, and N_{D0} are the impurity concentration, the ionised impurity and the non-inonised impurity at zero field, respectively. R_0 is the minimum LDD resistance when no freeze-out effect occurs, N_{D0}^+/N_D is the thermal equilibrium ionisation rate, and γ is the Chynoweth-like

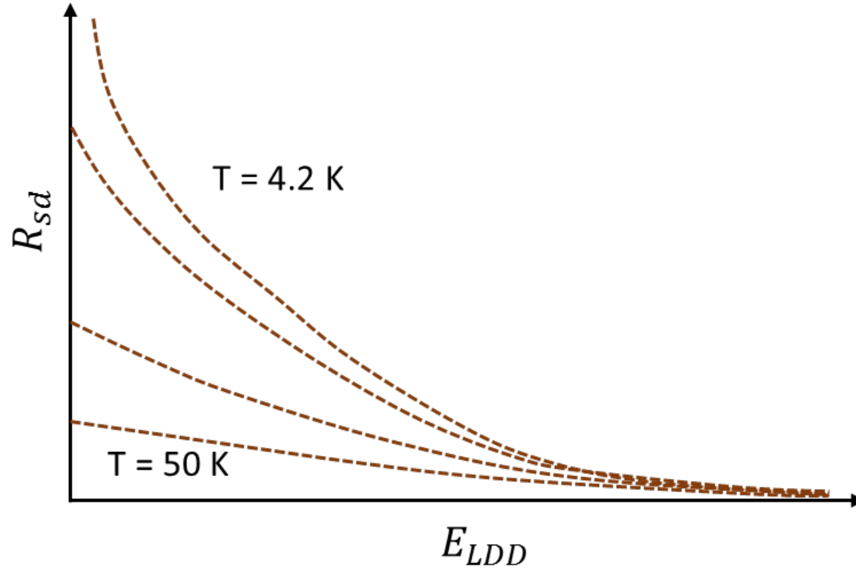


Figure 2.13: LDD series resistance R_{sd} versus electric field E_{LDD} (adapted from [10]

formula for the impurity ionisation rate as a function of electric field, determined as [82].

$$\gamma = \gamma_0 e^{-B/E_{LDD}}, \tag{2.37}$$

where γ_0 is a fitting parameter and B $\approx 1.33E_{d0}/(q\lambda)$ with λ being the hot-electron mean free path. It has been observed that a sufficient field can assist the freeze-out carriers in LDD region to be ionised and, hence, reduce this region resistance [10]. The so-called drain threshold voltage, V_{Td}, has been introduced as an activation quantity of the drain voltage required to assist impurity ionisation [70]. This V_{Td} is experimentally determined as an intersection of a linear fit to the drain current in the linear region and the V_{DS} x-axis (Figure 2.14). The existing V_{Td} could affect the I-V characteristic in the linear region at very low temperatures, leading to failure results when characterising the device in the linear region (at very low V_{DS}).

2.4 Reliability

A major concern of cryogenic CMOS circuits is reliability of the transistor [72, 83]. It has been widely agreed from several experimental results that lowering ionised carriers in the channel at cryogenic temperatures strongly affects device behaviour and its reliability [10, 17, 41, 84]. Two main factors employed in device reliability evaluation are hot carriers and device parameter variations.

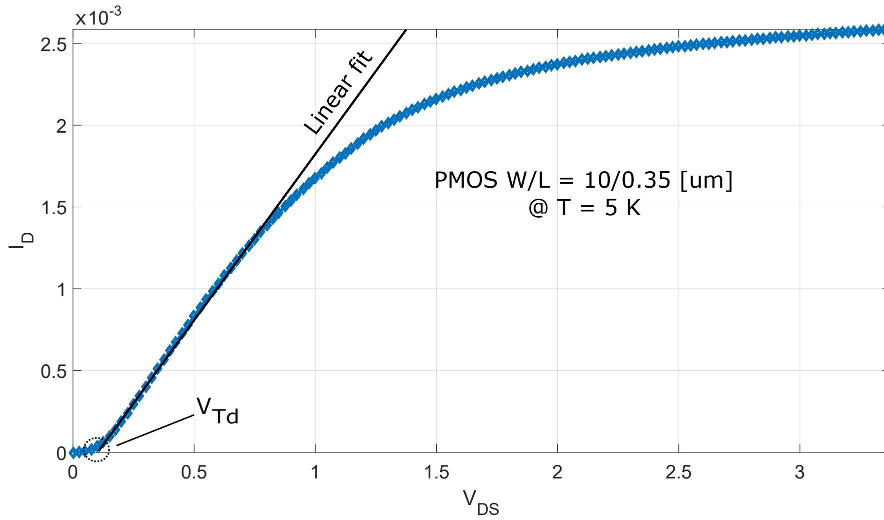


Figure 2.14: The drain threshold voltage

2.4.1 Hot carriers

When transistors operate in the inversion region, the electric field enhances carrier kinetic energy. If the field increases further, the carriers become “hot”. These hot carriers can be trapped in the silicon-oxide layer or get through to the gate, creating a leakage gate current [65]. This phenomenon could significantly degrade device lifetime.

Studies on this topic have revealed that hot carrier effects can be considered as a function of gate lengths and temperature [10, 65, 72]. At cryogenic temperatures, the number of hot carriers that reach the gate increase, due to decreases in lattice vibration (phonon scattering). That means the leakage gate current becomes aggravating, which in turn lead to failures in device performance [85]. Recent studies, however, have suggested that the increase in device degradation at low temperatures is mainly caused by scaled channel devices [65,72]. Therefore, LDD structures have been used to suppress the hot carrier effects in short channel devices [10, 24]. In addition, reducing the field by operating the MOS transistor with lower power supply could eliminate the need of LDD structure at low temperatures [65]. It is suggested that a compromise between the channel length and the operational temperature must be considered in order to obtain a reliable design for cryogenic applications [72].

2.4.2 Matching properties

Matching properties of transistors, especially for sub-micrometer devices, is a major concern in the design of accurate analog circuits. Mismatches of transistor parameters due to geometry effects could lead to circuit performance degradation and unexpected results. Several

studies have introduced models to determine variations of parameters and currents of MOS transistors [86–89].

The most common model used to evaluate variations of parameter ΔP between two transistors was proposed by Pelgrom et. al. in [86]

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \ , \tag{2.38}$$

where A_P is the area proportionality constant for parameter P, and S_P is the variation of parameter P with the spacing. D_x is the distance between two transistors, and W, L are width and length of transistor respectively. This model has been widely used to evaluate matching properties of MOS parameters such as the threshold voltage, the current factor β, mobility attenuation factors γ, and drain currents at room temperatures [87].

Besides parameter variations caused by distances and device's sizes, a random mismatch between two designed identical devices is also another issue in analog circuit designs. For example, a mismatch of drain currents from a differential pair will affect the input offset voltage and operations of the circuits [90]. In [87], Croon's et. al. proposed a model to predict the mismatch of drain currents based on variations of MOS parameters.

$$\sigma^2_{\left(\frac{\Delta I_D}{I_D}\right)} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{(\Delta V_T)} + \sigma^2_{\left(\frac{\Delta\beta}{\beta}\right)}, \tag{2.39}$$

where g_m is the transconductance, ΔV_T and $\Delta\beta$ are variations of the threshold voltage and the current factor.

For deep sub-micrometer devices, series resistance significantly affect device characteristics, therefore, variability of this parasitic component have to be considered in the mismatch model [91]. A model considering impact of series resistance was introduced in [92]

$$\sigma^2_{\left(\frac{\Delta I_D}{I_D}\right)} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{(\Delta V_T)} + (1 - G_d R_{sd})^2 \sigma^2_{\left(\frac{\Delta\mu}{\mu}\right)} + G_d^2 \sigma^2_{(\Delta R_{sd})}. \tag{2.40}$$

In Eq. (2.40), G_d is the channel conductance and ΔR_{sd} is the variation of series resistance. This formula was validated using advanced CMOS technology (20 nm) at room temperature [91].

Studies of device mismatch at low temperatures have not been reported thoroughly. Only a few works have investigated impacts of temperature on matching properties of MOS transistors. The work in [17] evaluated matching properties of 0.18 μm bulk CMOS devices at 77 K [17], whereas matching of 90 nm bulk NMOS was studied in [40] from 300 K down to 40 K. These works have reported that variabilities of transistor parameters become worse at low temperatures. To provide an extensive study of matching properties of bulk CMOS over the 5 - 300 K

temperature range, we will exclusively present this problem in Chapter 6.

2.5 Summary

A review of the electrical properties of Silicon CMOS devices, operated from room temperature down to liquid helium temperature, has been given. First, the operations and parameters of bulk CMOS have been reviewed. Then, summaries of cryogenic effects on the MOSFET characteristics are presented. The reliability of MOS devices were discussed in the last section of the chapter. It can be concluded that MOS devices enjoy a high performance at the intermediate cold temperature (above 77 K). However, in extremely cold environments (below 40 K), when carriers turn to strong freeze-out, a number of abnormal behaviours occur such as hysteresis and the kink phenomenon, which in turn degrades the reliability of the device and circuit performance.

Advantages of cryogenic CMOS circuits at low temperatures can be listed as below:

- Higher operation speeds due to increasing in carrier mobility and saturation velocities.
- Lower power dissipation as a result of decreases in parasitic components and the increase in subthreshold slope.
- Reduce circuit delay because of increased interconnection conductivities and decreased parasitic components.
- Elimination of latch-up due to a dramatic reduction in the gain of the parasitic bipolar transistor.
- Improved digital and analog circuit performance such as switching speeds, noise margins, and gain-bandwidth products.

Some major issues of cryogenic CMOS circuits at low temperatures:

- Anomalous behaviours such as the kink and hysteresis phenomenon.
- Hot carrier effects.
- Variability of device parameters and mismatch of the drain current.
- Lack of device models for circuit simulations.

Chapter 3

MOSFET parameter extractions

This chapter focuses on transistor parameter extraction including series resistance (R_{sd}), carrier mobility (μ) and its attenuation (θ) factor due to their importance in device modelling. Threshold voltage extraction and modelling are discussed in the next chapter.

This chapter begins with a discussion of existing methods for bulk CMOS parameter extraction at low temperatures. Limitations of conventional extraction methods are discussed before introducing a new approach to extract transistor parameters over the 5 - 300 K temperature range. The chapter then presents results from the proposed extraction method together with detailed comparisons with conventional methods. Finally, a summary is given in the last section. All detailed measurements are provided in Appendix A.

3.1 Introduction

Models cannot replicate exact behaviours of devices unless appropriate values are used for device parameters. Therefore, reliable extraction is important for device characterisation and device modelling.

Several methods have been introduced for MOSFET characterisation at room temperature [19,92–95] or at a particular temperature, i.e. 77 K [63,96,97]. However, a dedicated parameter extraction method for bulk CMOS devices, operating from room temperature down to liquid helium temperature, has not been previously reported.

Device modelling is particularly challenging for sub-micrometer bulk CMOS because the presence of series resistance and the degradation of carrier mobility cannot be ignored when extracting parameters. A detailed review of extraction methods for MOSFET series resistance and mobility degradation was reported in [19]. It was confirmed that existing methods were not able to extract source/drain series resistance for sub-micrometer bulk CMOS when the ambient

temperature was below 77 K [19, 63]. For example, a common total resistance method R_{tot} [98], which uses several devices of different channel length and assumes the source/drain series resistance is independent to V_{GS}, failed when applied to the p-channel device at 77 K [19].

The well-known Y-function method (Y = $I_D/\sqrt{g_m}$), when applied at a particular temperature - i.e. at liquid helium temperature [99], at liquid nitrogen temperature [100], or over a wide temperature range [101], assumes R_{sd} is either independent of gate voltage or channel length, resulting inaccurate in extraction results. Figure 3.1 illustrates this failure when applying the Y-function method to extract PMOS parameters at 5 K. In this experiment, I_D-V_{GS} characteristics were measured in the linear region with V_{DS} = 0.1 V. The figure highlights that the slope of theta (θ) with beta (β) becomes negative in the short channel (0.35 μm) when T = 5 K. That implies the source/drain series resistance has an unexpected negative value, which is physically an incorrect result.

A correction procedure for Y-function based technique is presented in [96] to reduce the impact of the series resistance at 77 K. This approach used a pair of long-short transistors and iteration method in R_{sd} approximation to extract device parameters. Although the study was able to obtain better results in comparison to the original, this technique is inaccurate because it assumes variations of the source/drain series resistance are less than one percent which is not always the case [20,91]. Another R_{tot} - $1/\beta$ technique [64], derived fromY-function and applied for nanometer channel devices, is similarly unable to extract parameters at low temperatures due to nonlinearity relations between R_{tot} and $1/\beta$ when the gate voltage changes (Figure 3.2).

Other extraction techniques lack accuracy because they do not take into account the dependent of R_{sd} to electrical effective channel length or mobility attenuation [93, 102]. As a result, they are unsuitable for parameters extraction at cryogenic temperatures [19].

In the next section, a new approach to extract MOSFET parameters at low temperatures is presented. The proposed approach was able to eliminate the effects of channel length reduction and minimise the impact of the series resistance. This allowed us to accurately estimate the source/drain series resistance and intrinsic parameters of sub-micrometer bulk MOSFETs over the 5-300 K temperature range.

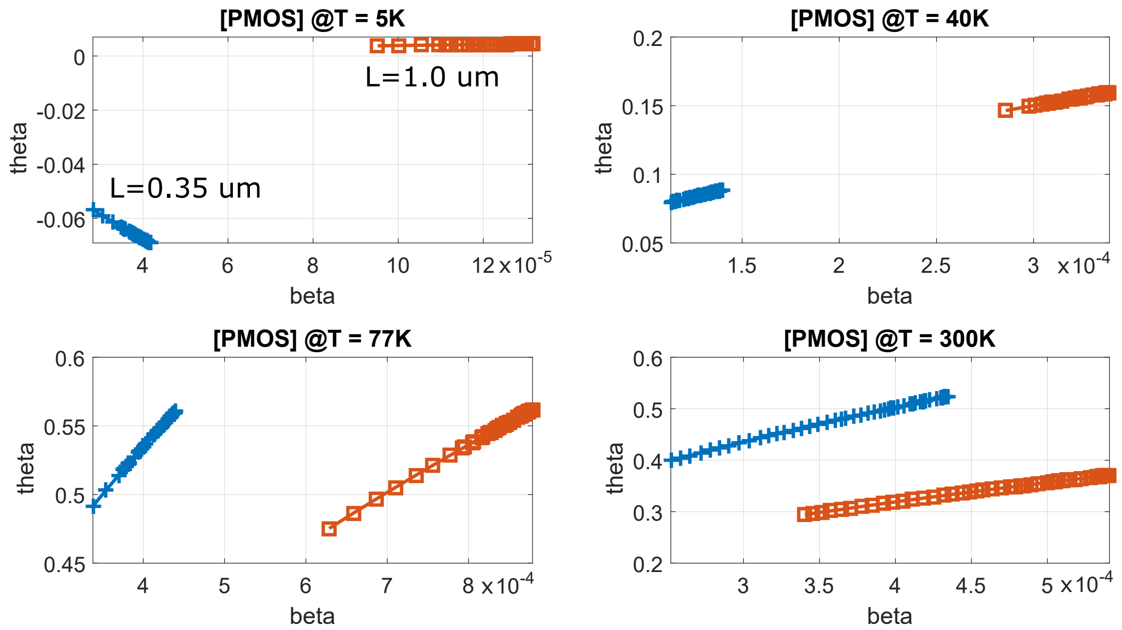


Figure 3.1: Y-function based method applied to extract R_{sd} of PMOS W/L = 10/0.35 (blue) and 10/1 (orange). R_{sd} is extracted from the slope of theta (θ) vs beta (β): $\theta = \theta_0 + R_{sd}\beta$. It failed to extract R_{sd} at 5 K since the slope turned to negative in case W/L = 10/0.35 (blue).

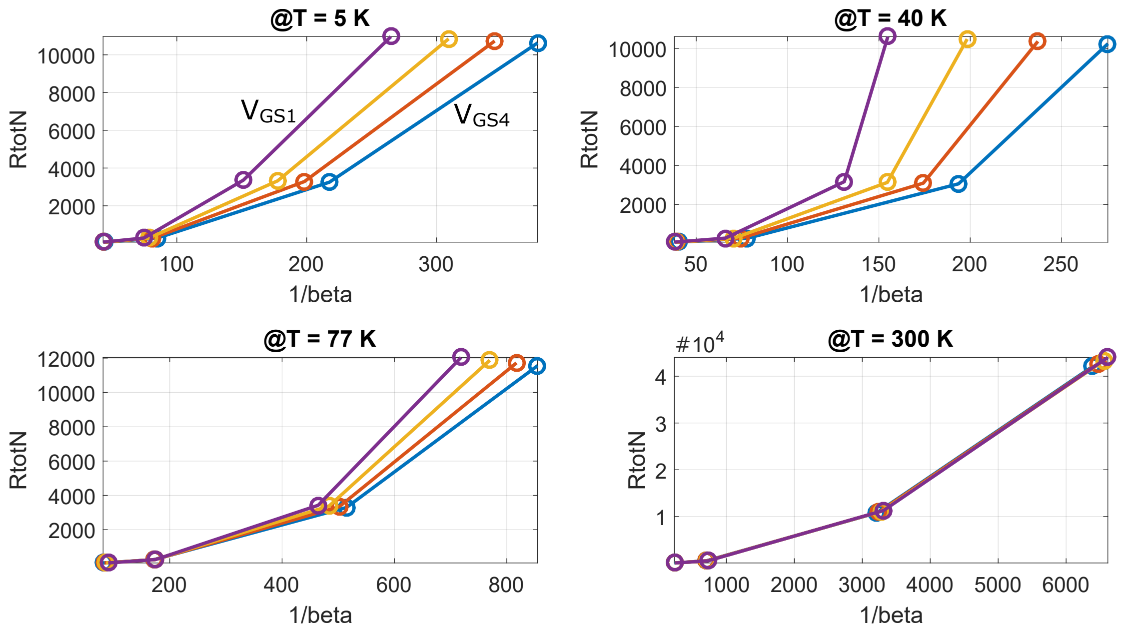


Figure 3.2: R_{tot} - $1/\beta$ method applied to extract R_{sd}. It was expected to obtain R_{tot} linearly proportional to $1/\beta$, and R_{sd} was extracted from the y-intercept. The figure clearly shows the relation between R_{tot} and $1/\beta$ is not linear when V_{GS} changes at low temperatures. The resulting R_{sd} cannot be determined.

3.2 A new parameter extraction approach

A new approach relies on the drain current model, presented in [101], which is applied for the strong inversion region ($V_{GS} > V_T$) of the drain current, I_D, operating in the linear regime ($V_{DS} \ll V_{GS} - V_T$). The intrinsic I-V characteristic of MOSFET is given in Eq. 3.1,

$$I_D = \mu_g C_{ox} \frac{W}{L} \frac{\theta^{n-2} V_{GST}^{n-1}}{1 + (\theta V_{GST})^{n-1}} V_{DS}^{'}. \tag{3.1}$$

In Eq. (3.1), W, L are the effective channel width and length, C_{ox} is the gate oxide capacitance, μ_g is a generalised mobility parameter related to the maximum effective mobility [101]. θ is the intrinsic mobility attenuation factor, and $V_{DS}^{'}$ is the effective drain-source voltage. V_{GST} = V_{GS} - V_T is the overdrive gate voltage, where V_{GS}, V_T are the gate voltage and the threshold voltage, respectively. The threshold voltage over a wide temperature range is obtained from [21] (see Chapter 4). The exponent n, which is related to characteristics of carrier mobility or carrier scattering mechanisms, varies from 2 to 3 corresponding to a temperature range of 300 K to 4.2 K [63, 100].

Taking into account the source/drain series resistance R_{sd}, and define

$$R_{ch0} = \frac{1 + (\theta V_{GST})^{n-1}}{\mu_g C_{ox} W \theta^{n-2} V_{GST}^{n-1}} \tag{3.2}$$

as normalised intrinsic channel resistance per unit length ($\Omega/\mu m$), the drain current is then rewritten as

$$I_D = \frac{1}{R_{ch0} L} \left(V_{DS} - R_{sd} I_D \right), \tag{3.3}$$

where V_{DS} is the extrinsic drain-source voltage. From Eq. (3.3), the total channel resistance, R_{tot} = V_{DS}/I_D can be determined from

$$\begin{aligned} R_{tot} &= R_{ch0}(L_m - \Delta L) + R_{sd} \\ &= R_{ch0} L_m + R_{sd} - R_{ch0} \Delta L, \end{aligned} \tag{3.4}$$

where L_m is the mask length, and ΔL is the channel length reduction. Eq. (3.4) shows that R_{tot} can be split into two parts: the channel resistance regarding the mask length (the first term) and the total series resistance (the second and third term).

Unlike [63, 100] where the source/drain resistance, R_{sd} is assumed constant, the series resistance in this method is considered a function of the gate voltage. This assumption has proven to be more accurate for bulk CMOS parameter extractions [64, 94, 103, 104]. For the LDD-type devices, the total series resistance must account for the LDD region which significantly changes

with the gate voltage and temperature. Moreover, the series resistance and channel reduction also vary with the channel length [93, 105]. Since R_{sd} and ΔL are interdependent, it is very difficult to separate their contributions towards the total series resistance for different channel lengths, as both temperature and gate voltage vary. However, based on physical device structure of bulk MOSFETs, a hypothesis can be proposed that the total series resistance, including contact resistance, source/drain diffusion resistance and resistance of LDD region, can be split into two components. This is shown as

$$R_{sd}^{*} = R_{sd0} + R_{sdL}, \tag{3.5}$$

where R_{sd0} is the series resistance which is independent of channel length variations due to V_{GST}, and R_{sdL} denotes variations of the series resistance to channel lengths and V_{GST}. Both R_{sd0} and R_{sdL} are functions of V_{GST} and temperature. Noting that the intrinsic overdrive gate voltage is assumed to be $V_{GST}^{'}$ = V_{GST} - $\frac{R_{sd}^{*}/2}{R_{tot}} V_{DS} \approx V_{GST}$ since V_{DS} is small (0.1 V) and $R_{tot} \gg R_{sd}^{*}/2$.

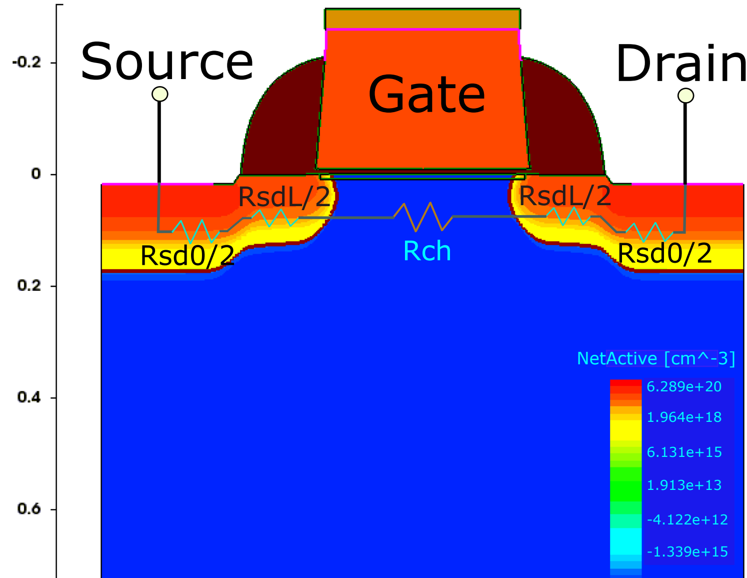


Figure 3.3: Series resistance in the channel

Using this, the replacement of the total series resistance in Eq. (3.4), R_{sd} - $R_{ch0}\Delta L$, by R_{sd}^{*} in Eq. (3.5), R_{tot} can be rewritten as

$$R_{tot} = R_{ch0}L_m + R_{sd0} + R_{sdL}. \tag{3.6}$$

3.2.1 Series resistance extraction

The core idea in this source/drain series resistance extraction technique relies on total resistance linear regression in which several devices of different mask channel lengths are employed. As analysed in the previous section, R_{sd0}, is independent of the mask channel length and only varies with V_{GST}. Therefore, with a set of devices of the same width, but different lengths, the total resistance can be separated into the channel resistance and the series resistance as followed

$$\begin{aligned} R_{tot,L_{12}} &= R_{tot,L_1} - R_{tot,L_2} \\ &= R_{ch0}L_1 + R_{sd0} + R_{sdL1} - (R_{ch0}L_2 + R_{sd0} + R_{sdL2}) \\ &= R_{ch0}L_{12} + R_{sdL1} - R_{sdL2}, \end{aligned} \tag{3.7}$$

where L_1, L_2 are the mask channel lengths, and L_{12} = L_1 - L_2. It is worth noting that, although this technique is based on linear regression which requires several mask channel lengths, it is possible to obtain similar results using a pair of different length transistors.

For a couple of long (L_1) and short channel (L_2) devices, it can assume that difference of the total resistance of long-short devices is much greater than the difference between R_{sdL1} and R_{sdL2}, or $R_{tot,L_{12}} \approx R_{ch0}L_{12} \gg R_{sdL1}$ - R_{sdL2}. In this case, Eq. (3.7) can be rewritten as

$$\begin{aligned} R_{tot,L_{12}} &\approx R_{ch0}L_{12}, \\ R_{ch0} &\approx \frac{R_{tot,L_{12}}}{L_{12}}. \end{aligned} \tag{3.8}$$

Therefore,

$$\begin{aligned} R_{ch0} &\approx \frac{R_{tot,L_1} - R_{tot,L_2}}{L_1 - L_2} \\ R_{sd0} &\approx R_{tot,L_1} - R_{ch0}L_1 - R_{sdL1}. \end{aligned} \tag{3.9}$$

Another assumption for a long channel device L_1 is $R_{tot,L1} \approx R_{ch0}L_1 + R_{sd0} \gg R_{sdL1}$. Thus,

$$R_{sd0} \approx R_{tot,L_1} - R_{ch0}L_1, \tag{3.10}$$

and R_{sdL} can be obtained from

$$R_{sdL1} = R_{tot,L_1} - R_{ch0}L_1, \tag{3.11}$$

From Eq. (3.10) and Eq. (3.11), the source/drain series resistance of difference channel devices can be obtained.

3.2.2 MOSFET intrinsic parameter extractions

The intrinsic MOSFET parameters, mobility μ_g and mobility attenuation factor θ, can be extracted from the normalised intrinsic channel resistance R_{ch0}. Eq. (3.2) is rewritten as

$$R_{ch0} = \frac{1}{\mu_g C_{ox} W \theta^{n-2}} \left(\frac{1}{V_{GST}^{n-1}} + \theta^{n-1} \right), \tag{3.12}$$

or,

$$R_{ch0} = \frac{p_1}{V_{GST}^{n-1}} + p_2, \tag{3.13}$$

where p_1, p_2 are fitting coefficients. When temperature varies from 300 K down to 4.2 K, n takes a value between 2 to 3. The coefficients from the best fitted R_{ch0} versus V_{GST} while varying n and temperatures reveal the value of n and θ. μ_g can be obtained from R_{ch0} after n and θ are determined. The effective mobility, μ_{eff}, is calculated, using the method described by Emrani et al. [101]:

$$\mu_{eff} = \mu_g \frac{(\theta V_{GST})^{n-2}}{1+(\theta V_{GST})^{n-1}}. \tag{3.14}$$

3.3 Experimental Details

The MOS transistors used in this study were fabricated in the Austrian MicroSystems 0.35 μm CMOS. To extract source/drain series resistance and MOS parameters in linear region, I_D-V_{GS} curves were taken at a fixed V_{DS} of 0.1 V. In this work, 64 transistors for each same-size device with dimensions W = 10 μm, L = 0.35, 1, 5, and 10 μm were examined. Detailed experimental setup, equipment and test circuits are presented in Chapter 6.

3.4 Results and Discussions

In order to validate the proposed approach, it is applied to extract parameters and series resistance of 0.35 μm bulk CMOS over a wide range of temperature, and then compared it to the existing methods. Extraction results of the source/drain series resistance from 5 K to 300K are shown in Figure 3.4 for both PMOS and NMOS W/L = 10/0.35 [μm]. It distinctly shows that series resistance increases as temperature decreases.

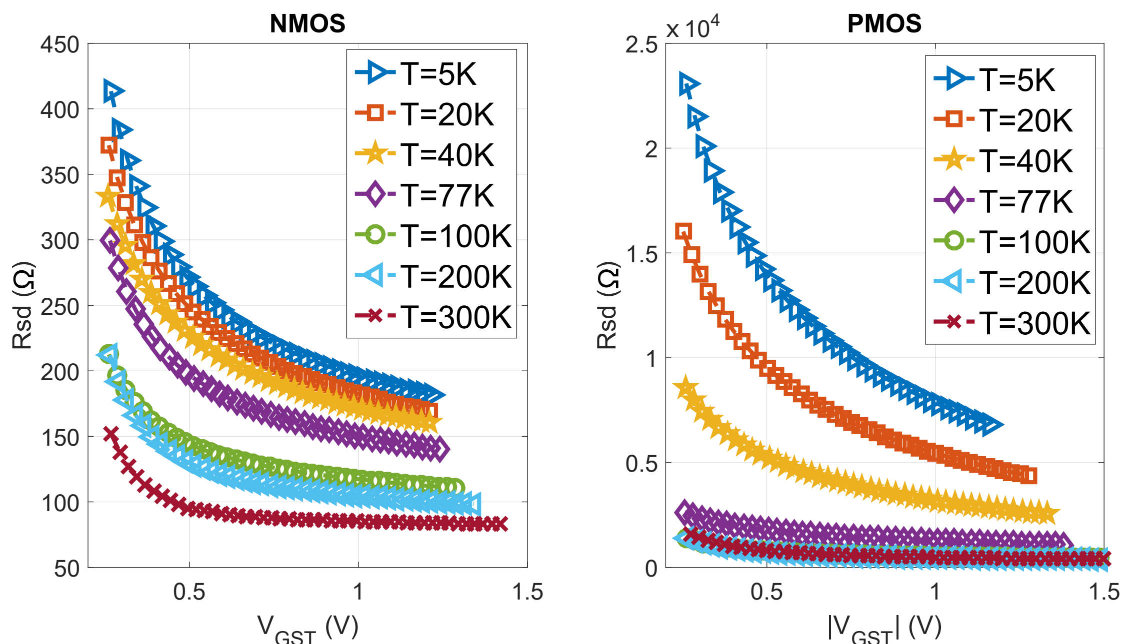


Figure 3.4: The source/drain series resistance of NMOS and PMOS W/L = 10/0.35 μm at different temperatures.

Comparisons between the extracted series resistance and results from conventional total resistance method [98] are depicted in Figure 3.5 for NMOS and Figure 3.6 for PMOS. It is worth noting that the conventional method assumes channel reduction ΔL is a constant and R_{sd} is a function of V_{GST}.

Results show the proposed approach fits the measured data better than the existing method, which deviates from the measurements, mostly at low V_{GST} and low temperatures. Figure 3.7 and 3.8 show different values (in percentage) extracted from the proposed approach and the conventional total resistance method. More specifically, extractions for both PMOS and NMOS from the new approach and the existing method are similar at room temperature, however the old model loses accuracy as temperature decreases.

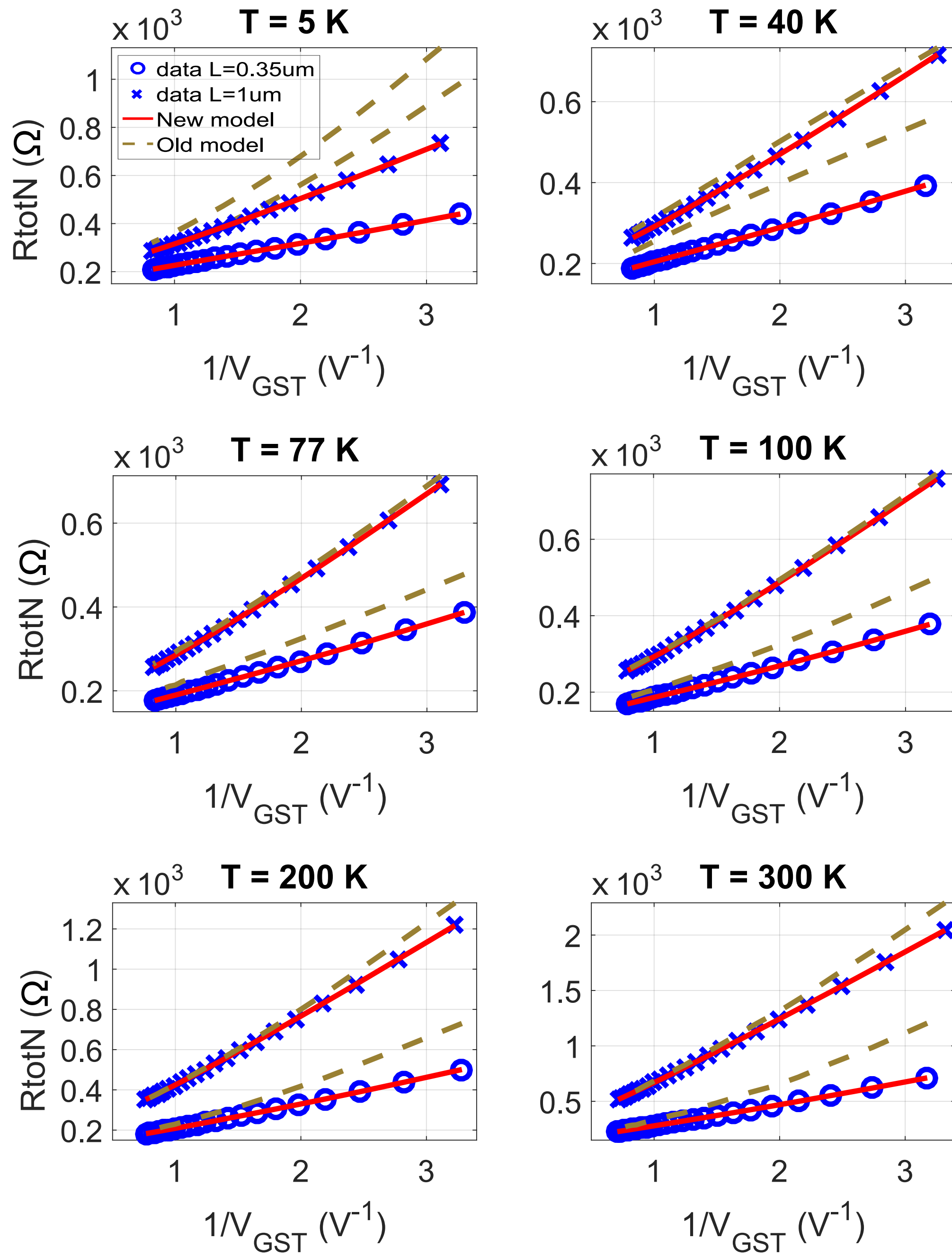


Figure 3.5: The total resistance of NMOS W = 10 μm, L = 1, 0.35 μm: measured data (symbols), new extraction (lines), and conventional model (dashed lines).

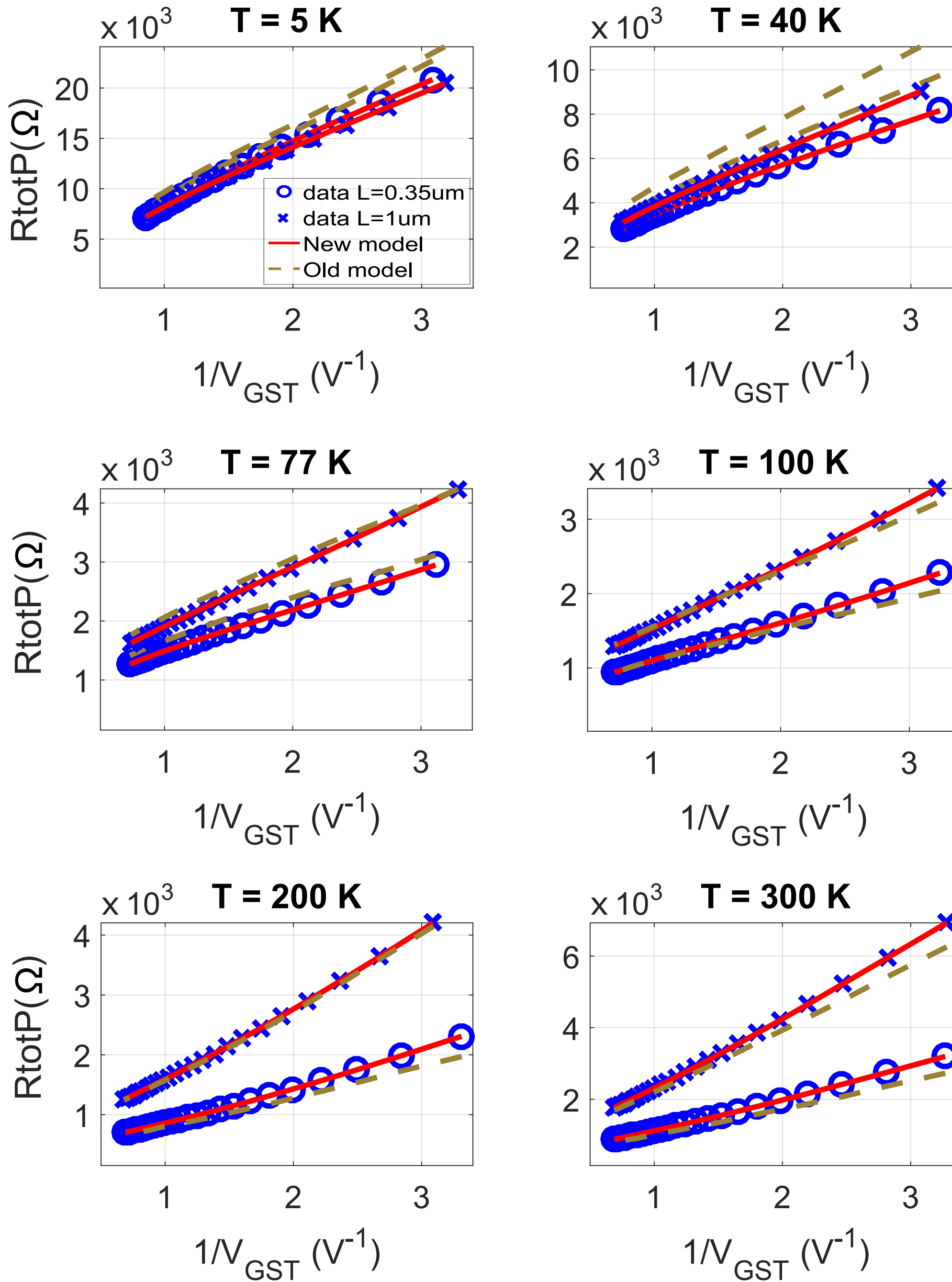


Figure 3.6: The total resistance of PMOS W = 10 μm, L = 1, 0.35 μm: measured data (symbols), new extraction (lines), and conventional model (dashed lines).

It also can be seen that extraction results from short channel transistors (L = 0.35 μm) are not as effective as compared to longer channel transistors (L = 1 μm) as shown in Figure 3.5 and Figure 3.6. That is because of impacts of temperature on the LDD region resistance [82], which in turn significantly change the series resistance. A comparison of series resistance extracted from our method and the Y-function method at room temperature is also presented in Table

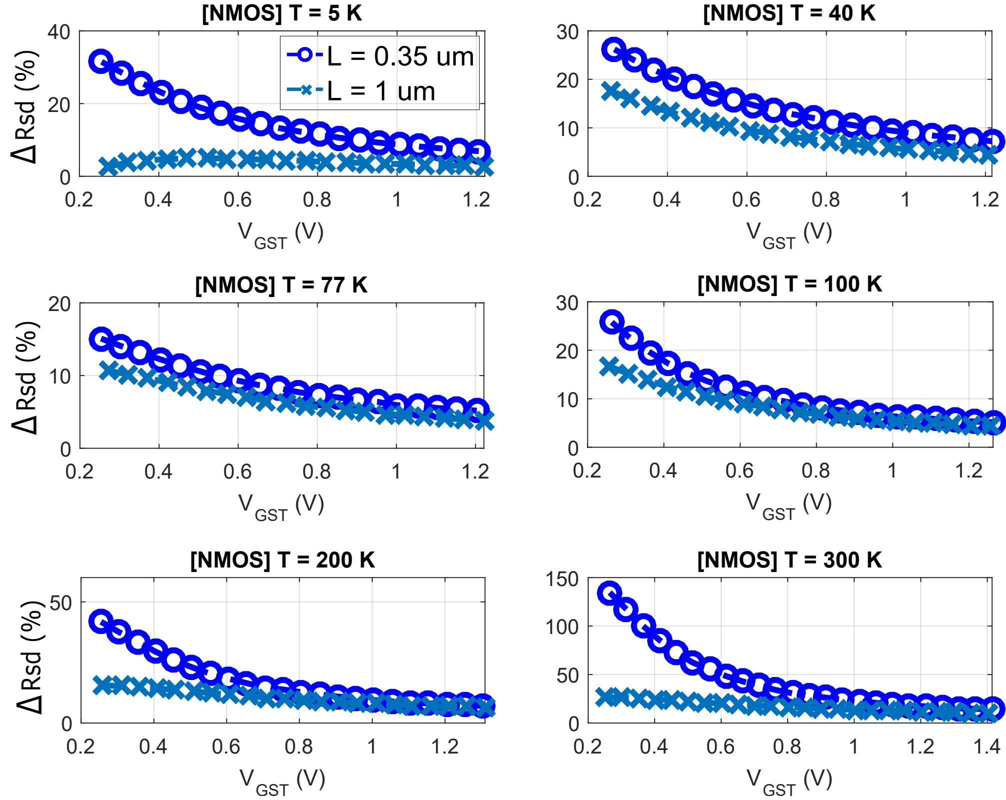


Figure 3.7: Differences between the proposed approach and the old method $\Delta R_{sd} = 100 * \frac{|R_{sd,new} - R_{sd,old}|}{R_{sd,new}}$ (%).

3.1. Note that the Y-function method here assumes R_{sd} is V_{GST} dependent and channel length independent.

Table 3.1: Comparison results from the new method and the Y-function method at 300 K

R_{sd} @ V_{GST} = 1.2 V (Ohm)		**NMOS**	**PMOS**
New method	W/L = 10/1	102	395
	W/L = 10/0.35	84.1	398
Y-function method		94.1	378

In this approach, mobility is assumed to be independent of channel length when L is greater than 100 nm [106]. Therefore, the accuracy of this approach primarily depends on the error in the R_{ch0} approximation. Our empirical results (Figure 3.9) suggest that, L_{12} should be greater than 5 μm for the best extraction results.

Differences between R_{sd} extracted from linear regression when using several gate-mask-length and from long-short (i.e. $L_{12} = 9$ μm) pair devices are shown in Figure 3.10. It shows that

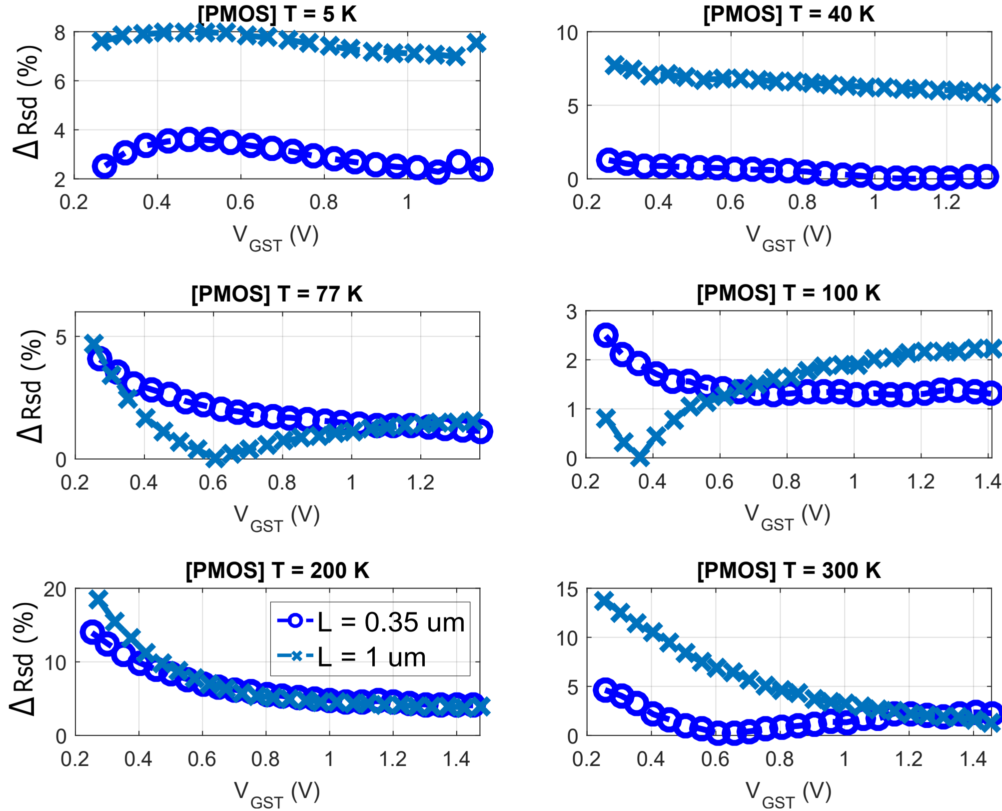


Figure 3.8: Differences between the proposed approach and the old method $\Delta R_{sd} = 100 * \frac{|R_{sd,new} - R_{sd,old}|}{R_{sd,new}}$ (%).

results are similar as differences are very small (less than 3.1%) over all examined temperatures. Thus the proposed approach can be applied to several channel lengths without using an array of transistors as required in the linear regression approach.

Mobility μ_g and its attenuation factor θ are calculated from the best fitting coefficients of R_{ch0} in Eq. (3.12). It is worth noting that to keep the physical meaning of n [99], its fitting boundaries are referenced from [101]. The maximum fitting error (adjusted R-squared) is less than 0.3% for all type of transistors over the 5-300 K temperature range. Extracted parameters are summarised in Table 3.2.

The results of mobility at room temperature, μ_g=376 cm^2/Vs (NMOS) and μ_g=123 cm^2/Vs (PMOS), are very close to the values from foundry (370 and 126, respectively). The effective mobility μ_{eff}, obtained from Eq. (3.14), is plotted in Figure 3.11.

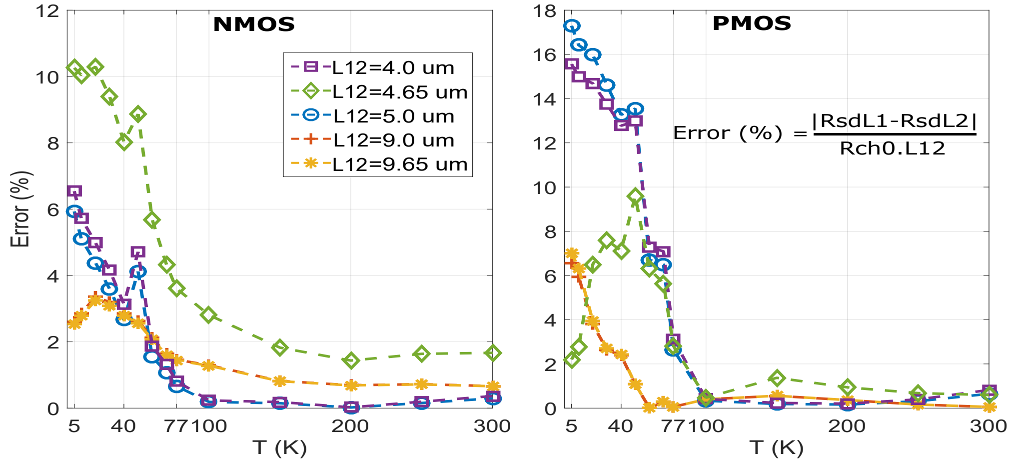


Figure 3.9: Error in R_{ch0} approximation

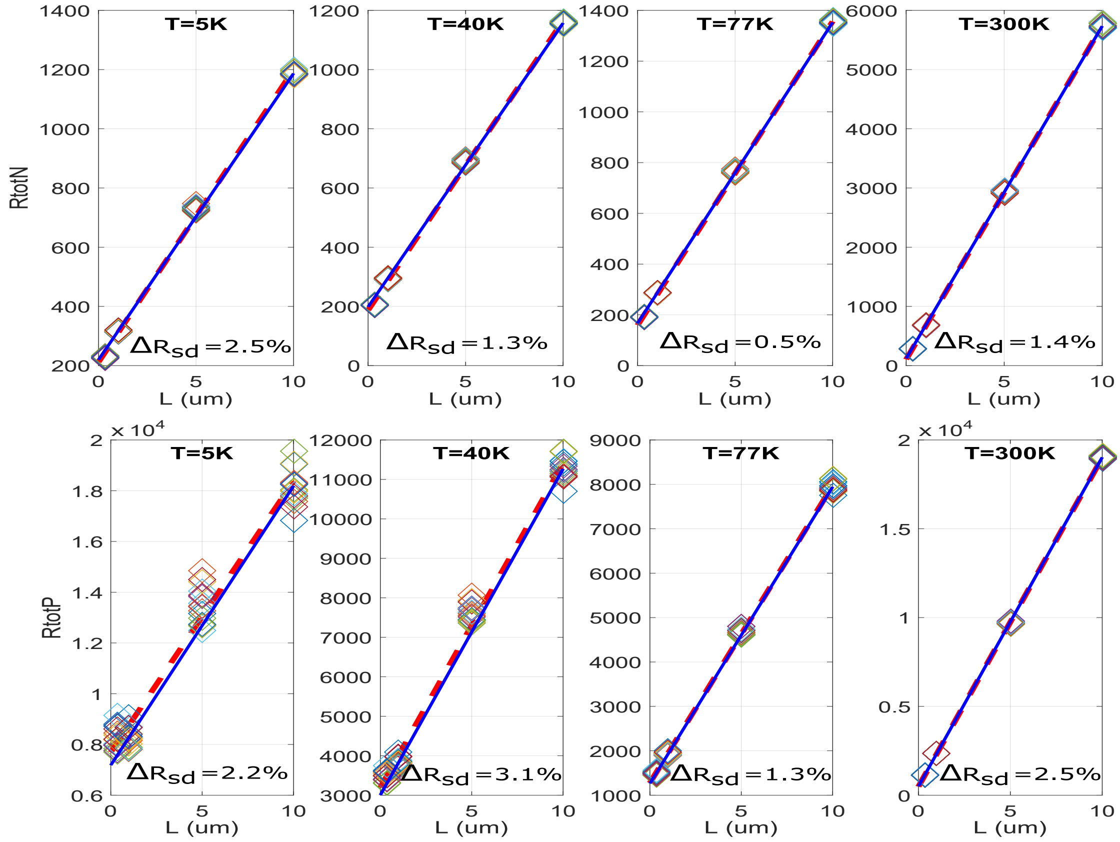


Figure 3.10: Series resistance using linear regression

At 100 K, the effective mobility extracted from the new approach and from [98] show similar results for the same device size (about 1500 cm^2/Vs in NMOS and 300 cm^2/Vs in PMOS). Our results are also consistent with results in [101]. It shows that mobility increases with decreasing

temperature. Carrier mobility in n-type devices saturated at very low temperatures (below 20 K) while it reached the peak at 77 K in the p-type channel, then dropping down below that temperature. The difference in n-type and p-type device behaviour can be explained by the different doping levels in the substrate and the n-well which leads to the strong freeze-out of carriers occurring at different temperatures. Another reason is because the mobility property of electrons (in the substrate) and holes (in the n-well) are different.

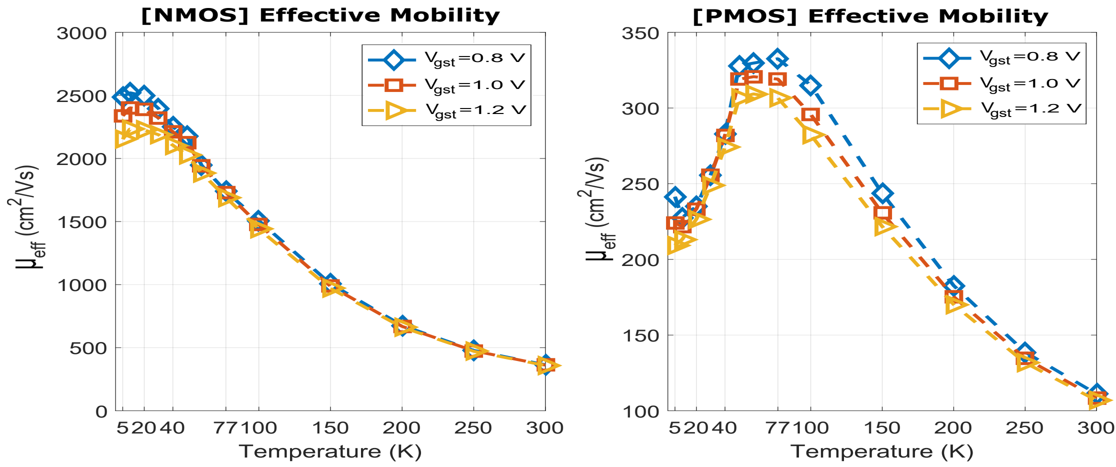


Figure 3.11: Effective Mobility at different temperatures and V_{GST}.

Table 3.2: MOSFET parameters

T (K)	5	40	60	77	100	200	300
n	3	3	2.75	2.5	2.1	2	2
NMOS							
θ (V^{-1})	1.48	1.2	0.96	0.72	0.28	0.06	0.04
μ_g (cm^2/Vs)	5068	4502	3868	3291	2089	708	376
PMOS							
θ (V^{-1})	1.58	1.13	1.11	0.99	0.63	0.25	0.13
μ_g (cm^2/Vs)	498	568	653	638	499	220	123

3.5 Summary

This chapter has briefly presented an overview of methods applied for bulk CMOS parameter extractions at cryogenic temperatures. A new approach to extract the series resistance and MOSFET parameters, which can be used for temperatures ranging from 300 K down to liquid

helium temperature, has been introduced. This new approach provides a simple, yet reliable technique for MOSFET parameter extraction over a wide temperature range. In particular, this approach eliminates the effect of the channel length reduction in the extraction procedure and takes into account the dependence of series resistance on gate voltage V_{GS} as well as channel length variations. Altogether, results from the new approach are consistent with the conventional methods at room temperature, but more importantly, they produce reliable results at very low temperatures.

Chapter 4

Low temperature threshold voltage model

This chapter presents an enhanced threshold voltage model for MOSFETs which operates from room temperature down to liquid helium temperature. First, a review of threshold voltage models for low temperature is briefly presented. Introduction of the proposed threshold voltage model is then presented. Next, impacts of short channel effects are discussed. Detailed measurements and threshold voltage extraction are provided in the next section. Results of the new model compared to the existing model are given and discussed before the summary in the last section.

Results in this chapter have been reported in Microelectronic Reliability [21].

4.1 Introduction

Threshold voltage is one of the key parameters in conventional MOSFET models, widely used in both simple MOS models (i.e. level 1) [24] and compact models such as BSIM model [29] or EKV model [35]. In MOSFET models, this parameter is used to distinguish transistor operations between the non-saturation and saturation regions. It also acts as a key quantity in MOSFET circuit design and serves as a quality control indicator for evaluating device reliability [107]. As mentioned in Chapter 2, several works have reported the change in the threshold voltage when temperature decreases. This is mainly due to the change of Fermi potential [9, 16, 18,24,28,41,47,54,75]. Some attempts have been made to create low-temperature MOS models, in which the threshold voltage at room temperature was replaced by its cold value [47, 54], or by fitting polynomial functions [16, 18]. Models devised for a specific temperature may need to be characterised at that temperature, and often do not provide insight into the device behaviour

over a wide temperature range. In addition, the complexity of the fitting function needs to be considered to achieve high computational efficiency. Therefore, a simplified threshold voltage model that faithfully accounts for wide changes in temperature should be developed.

The next section presents the first threshold voltage model for bulk CMOS transistors over the 5–300 K temperature range. The proposed model is derived from a simplified Fermi potential formula, which takes into account the freeze-out effect, and the external field-assisted ionization [21].

4.2 Temperature dependencies of Threshold voltage

4.2.1 N-channel devices

Chapter 2 shows that threshold voltage of a long channel NMOS operating in strong inversion regime is determined from (Eq. (2.19) is rewritten here for reference)

$$V_{T0} = |\phi_F| - \phi_{gate} - \frac{Q'_0}{C'_{ox}} + \gamma\sqrt{2|\phi_F|}\ . \tag{4.1}$$

As aforementioned, ϕ_{gate} and $\frac{Q'_0}{C'_{ox}}$ can be considered as temperature independence, therefore, in Eq. (4.1), ϕ_F is the main temperature dominator in variations of the threshold voltage.

The conventional formula used to calculate the Fermi potential is $\phi_F = \frac{kT}{q}\ln(\frac{N_A}{n_i})$, where k is Boltzmann's constant, q is the elementary charge, n_i is the intrinsic concentration and N_A is the substrate doping concentration which is assumed equal to the ionized acceptor concentration N_A^- at room temperature [14]. However, for a wide temperature range and especially at low temperatures where N_A^- is no longer equal to N_A due to the freeze-out effect (Fig. 4.1(a)). Therefore, to represent the temperature dependence in calculating ϕ_F, incomplete ionisation N_A^-, Eq. (2.2), must be used. In addition, n_i, a function of temperature [14] also have to taken into account.

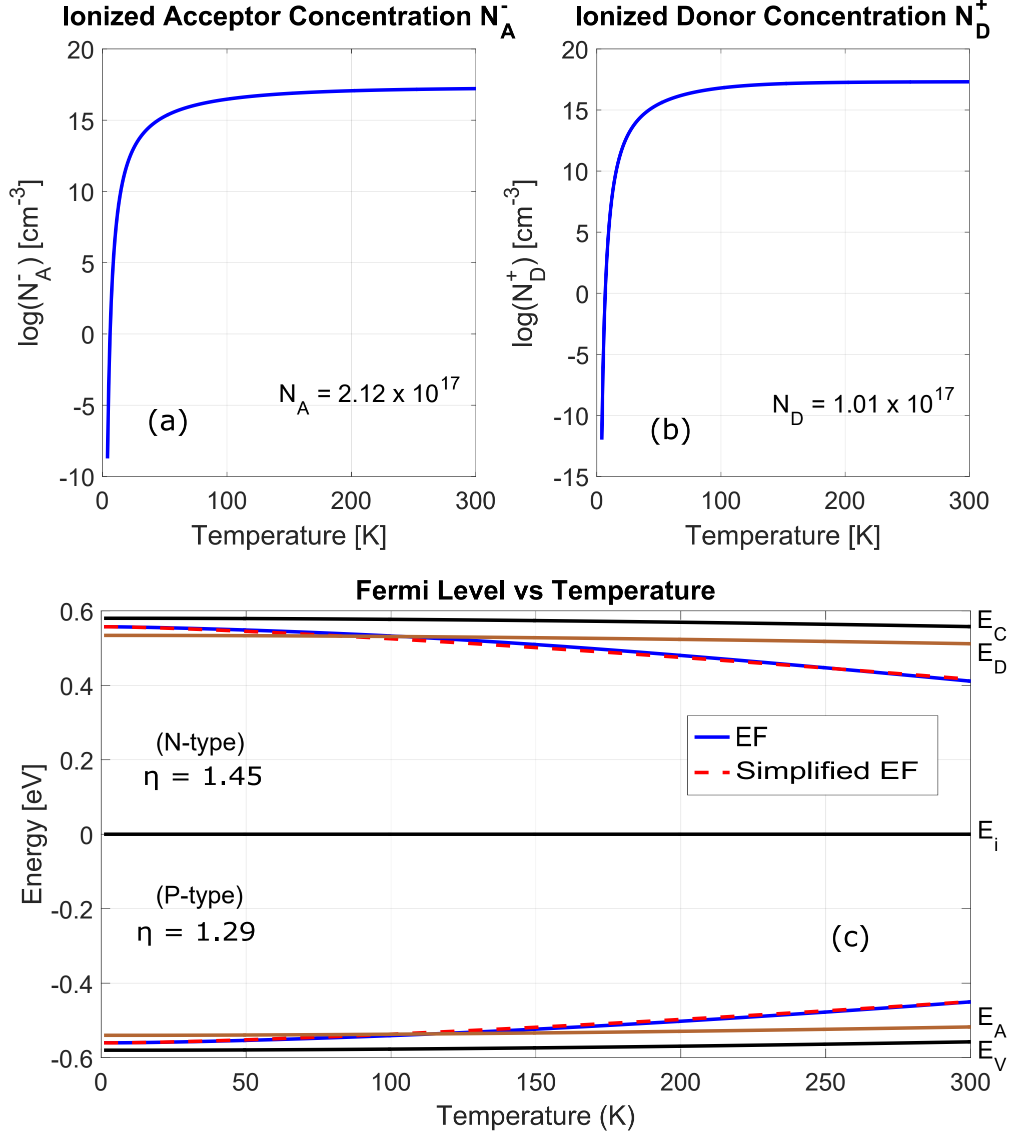


Figure 4.1: (a) Ionized Acceptor concentration N_A^-, (b) Ionized Donor concentration N_D^+, and (c) Simplified model of Fermi energy E_F.

In this work, the Fermi potential ϕ_F, used in Fermi-Dirac statistics, is derived from the Fermi energy instead of carrier concentrations as $\phi_F = \frac{E_F - E_i}{q}$, where E_i is the intrinsic energy and E_F is the Fermi energy [24]. Taking into account the freeze-out of acceptors and solving for the Fermi energy in the charge neutrality condition for p-type material [9], the Fermi potential ϕ_F is calculated as shown in Eq. (2.3). The expression is transcribed here for reference.

$$\phi_F = \frac{E_A + E_V}{2q} - \frac{kT}{2q} ln\left(\frac{N_A}{4N_V}\right) - \frac{kT}{q} sinh^{-1}\left(\sqrt{\frac{N_V}{16N_A}} e^{-(E_A - E_V)/2kT}\right), \tag{4.2}$$

where $N_V \approx 2.0015\times10^{15}\times T^{3/2}$ is the effective density of states in the valence band for Si, and E_A and E_V are the energy level of acceptor and valence band, respectively [14]. Note that all energy levels are referenced to the intrinsic energy.

In order to make ϕ_F less computationally expensive and facilitates incorporation it into SPICE models, Eq. (4.2) can be simplified by introducing a fitting parameter, η, and neglecting the inverse hyperbolic sine term to obtain

$$\phi_F \cong \frac{E_A+E_V}{2q} - \frac{\eta kT}{2q} ln\left(\frac{N_A}{4N_V}\right) . \tag{4.3}$$

The difference between the simplified ϕ_F in Eq. (4.3) versus the one in Eq. (4.2) is less than one percent. A plot of ϕ_F or E_F referenced to E_i = 0 is shown in Fig. 4.1(c).

The other factor that must be taken into account at low temperatures is field-assisted or Poole-Frenkel ionization [25]. When a field is applied, the potential barrier moves lower meaning that the field assists carrier ionization. The reduction of the potential barrier due to an applied field can be determined as ΔU=2$\sqrt{\frac{qF}{\varepsilon_{Si}}}$, where F is the field strength, and ε_{Si} is the permittivity of silicon [25]. Based on the Poole-Frenkel theory, $\Delta\phi_G$ can be defined as the potential reduction caused by the external field that relates to a gate voltage variation ΔV_G. The field caused by ΔV_G can be written as F=$\Delta V_G/T_{ox}$. Therefore, $\Delta\phi_G$ can be given as

$$\Delta\phi_G = 2\sqrt{\frac{q\Delta V_G}{\varepsilon_{Si}T_{ox}}} , \tag{4.4}$$

where T_{ox} is the gate oxide thickness.

Since low temperatures lead to freeze-out of carriers, a sufficient field is required to assist the ionization of trapped carriers, depletion region formation, and channel formation. A formula to calculate the potential change required to ionize and form the channel can be proposed as follows

$$\frac{\Delta\phi_G}{kT} = \beta\left(\frac{\phi_{AF0}}{kT_0} - \frac{\phi_{AF}}{kT}\right) , \tag{4.5}$$

where β is an empirical constant which is proportional to the amount of potential reduction with respect to the potential at room temperature. Here, ϕ_{AF} is the activation potential for acceptors defined as

$$\phi_{AF} = \frac{E_A - mE_F}{q} , \tag{4.6}$$

where m is a freeze-out coefficient corresponding to the strong freeze-out effect (this point will be discussed later). Also, ϕ_{AF0} is the activation potential at room temperature T_0. Eq. (4.5) shows the amount of potential required to assist carrier ionization, and form the channel at the

level of carrier concentration for room temperature.

From (4.4) and (4.5), ΔV_G corresponding to the potential reduction $\Delta\phi_G$ can be determined as

$$\Delta V_G = \frac{\varepsilon_{Si} T_{ox}}{4q} \beta^2 \left(\phi_{AF0} \frac{T}{T_0} - \phi_{AF} \right)^2 . \tag{4.7}$$

Therefore, the threshold voltage formula for a wide range of temperatures can be rewritten as

$$V_{T0} = |\phi_F| - \phi_{gate} - \frac{Q'_o}{C'_{ox}} + \gamma\sqrt{2|\phi_F|} + \Delta V_G . \tag{4.8}$$

4.2.2 P-channel devices

Similar to N-channel devices, the threshold voltage model of P-channel devices over 5-300 K temperature range can be written as

$$V_{T0} = \phi_F - \phi_{gate} - \frac{Q'_0}{C'_{ox}} + \gamma\sqrt{2\phi_F} + \Delta V_G , \tag{4.9}$$

where

$$\phi_F \cong \frac{E_D + E_C}{2q} + \frac{\eta k T}{2q} ln \left(\frac{N_D}{2N_C} \right) . \tag{4.10}$$

In Eq. (4.10), E_D and E_C are the energy levels of donors and conduction band, respectively [14]. $N_C \approx 5.4078 \times 10^{15} \times T^{3/2}$ is the effective density of states in the conduction band for Si. The ionized donors are given as $N_D^+ = \frac{N_D}{1+2e^{(E_F - E_D)/kT}}$ [14], where N_D is the donor concentration (Fig. 4.1(b)).

The additional field-assisted ionization ΔV_G for the P-channel devices also follows the proposed formula in Eq. (4.7) with the activation potential ϕ_{AF} given as

$$\phi_{AF} = \frac{E_D - mE_F}{q} . \tag{4.11}$$

Note that the values of η, β, and m for P-type and N-type are different (see the Results section).

4.3 Short channel effects

Effects of short channel on device characteristics are conventionally incorporated into the threshold voltage model [24]. As shown in Chapter 2, device dimensions significantly affect

the threshold voltage due to several phenomena such as charge sharing effects and non-uniform doping concentration effects.

At room temperature, models to predict the short channel effects have been introduced in Eq. (2.21). At low temperature, these effects are still present and must be modelled. For example, the charge sharing effect, which depends essentially on the depletion layer width, weakly varies when the temperature is above 77 K [41] but it may strongly impact the threshold voltage at very low temperature due to carrier freeze-out [25]. For simplicity, an empirical function $f_{SC}(T)$ to fit the geometry effects on the threshold voltage over a wide temperature range can be employed as follows:

$$f_{SC}(T) = \left(1 + sgn(\phi_F(T))\frac{\phi_F(T)}{\phi_F(T_c)}\right)\delta_{VT} \ , \tag{4.12}$$

where ϕ_F is the Fermi potential (positive for PMOS - Eq. (4.10), negative for NMOS - Eq. (4.3)), and δ_{VT} is a fitting parameter such that $f_{SC}(300K)$ = 1. T_C -the critical temperature (100 K), is empirically chosen at a point when the short channel effects are negligible (i.e. $f_{SC}(T_C)$ = 0). An extensive study on short channel effects at very low temperature is required to fully understand this phenomenon. Nevertheless, the presented fitting function Eq. (4.12) calculated from the proposed ϕ_F and the short channel effects at room temperature can predict the impact of such effects with temperature.

The threshold voltage with short channel effects is therefore given as

$$V_T = V_{T0} + \Delta V_T \times f_{SC}(T) \ . \tag{4.13}$$

4.4 Experimental setup and V_T extraction

The NMOS and PMOS transistors used in this study were fabricated in the Austrian MicroSystems 0.35 μm CMOS. Channel lengths of tested transistors vary from 0.35 to 10 μm and the width is 10 μm. Detailed experimental setup, equipment and test circuits are presented in Chapter 6.

I-V curves were taken using pulsed measurement (duty cycle is 10% out of a 5 ms period) to minimise the self-heating effect. To eliminate effects of series resistance on threshold voltage extraction at low temperatures, the G_m-Max method is used [107, 108]. I_D-V_{GS} curves measured in linear region with fixed V_{DS} = 0.1 V. Using Eq. (2.9) with α = 1, the threshold voltage is calculated as below,

$$
\begin{aligned}
I_D &= \mu C_{ox}\frac{W}{L}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS},\\
g_m &= \frac{\partial I_D}{\partial V_{GS}}
\end{aligned}
\tag{4.14}
$$

and,

$$
V_T = V_{GS,@g_mMax} - \frac{V_{DS}}{2}. \tag{4.15}
$$

Eq. (4.15) shows that threshold voltage is determined as the gate voltage at which the derivative as the gate voltage at which the derivative of the transconductance is a maximum. Its origin can be understood by using the simple MOSFET model, i.e. Eq. (4.14), where I_D = 0 when $V_G < V_T + V_D/2$, and I_D is proportional to V_G when $V_G > V_T + V_D/2$. With this assumption, $\partial I_D/\partial V_{GS}$ will become infinity (reach the maximum value in practice) at $V_G = V_T + V_D/2$. The term $V_{DS}/2$ is used to obtain a better surface potential approximation in strong inversion regime [24]. Repetitions in I-V measurements, conducted to verify the accuracy of the measurement, showed that the maximum variation from 30 repetitions is less than 0.2% (about 1 mV) at the examined temperatures. The mean value of the threshold voltage was taken from 64 extracted data with the maximum standard deviation is less than 10 mV. The threshold voltage of NMOS and PMOS extracted at temperatures from 5 K to 300 K are presented in Table 4.1

Table 4.1: V_T extraction at different temperatures

V_T (V)	**Temperature (K)**								
	5	20	40	77	100	150	200	250	300
NMOS									
W/L=10/10	0.762	0.763	0.765	0.735	0.713	0.663	0.610	0.555	0.506
W/L=10/5	0.754	0.754	0.750	0.727	0.709	0.665	0.615	0.562	0.514
W/L=10/1	0.750	0.749	0.743	0.729	0.717	0.682	0.640	0.594	0.549
W/L=10/0.35	0.740	0.739	0.734	0.722	0.711	0.682	0.645	0.604	0.560
PMOS									
W/L=10/10	1.349	1.298	1.242	1.194	1.158	1.063	0.961	0.862	0.775
W/L=10/5	1.338	1.289	1.234	1.188	1.155	1.061	0.960	0.861	0.776
W/L=10/1	1.310	1.272	1.225	1.171	1.139	1.051	0.951	0.854	0.770
W/L=10/0.35	1.289	1.259	1.215	1.153	1.116	1.025	0.923	0.827	0.754

4.5 Results and Discussions

The variation of the threshold voltage of a long channel NMOS as a function of temperature is shown in Fig. 4.2. The fitting parameter η in the Fermi potential model is 1.29, $\beta = 10.365$,

and the freeze-out coefficient m in Eq. (4.6) is 1 over the 5-300 K temperature range. The other parameters such as T_{ox}, C_{ox}, ϕ_{gate}, Q_o' etc. are taken from AMS C35 process parameter [109] and calculated from extraction at room temperature. It is clear that the proposed model V_{T0} (Eq. (4.8)) provides a better fit to the experimental data than the conventional model (Eq. (4.1)) which is only valid at room temperatures.

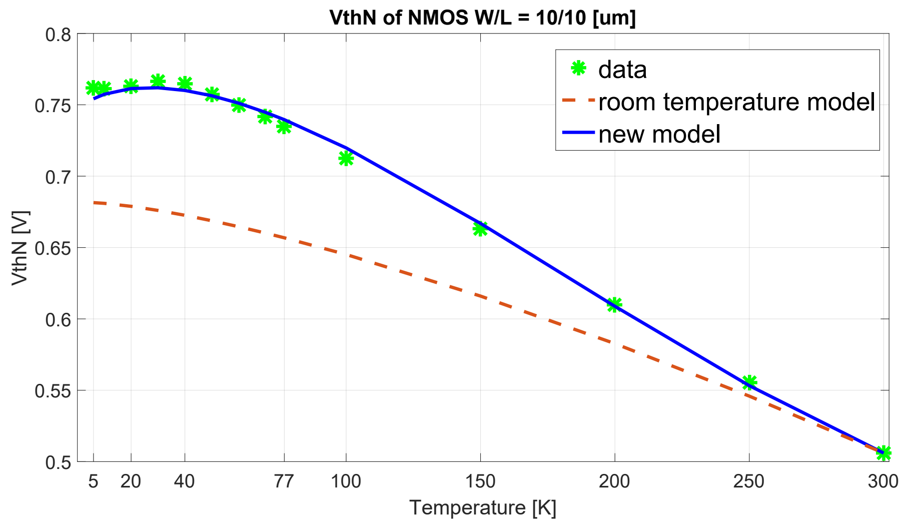


Figure 4.2: The temperature dependence of V_{T0} of NMOS: new model, conventional model, and experimental data

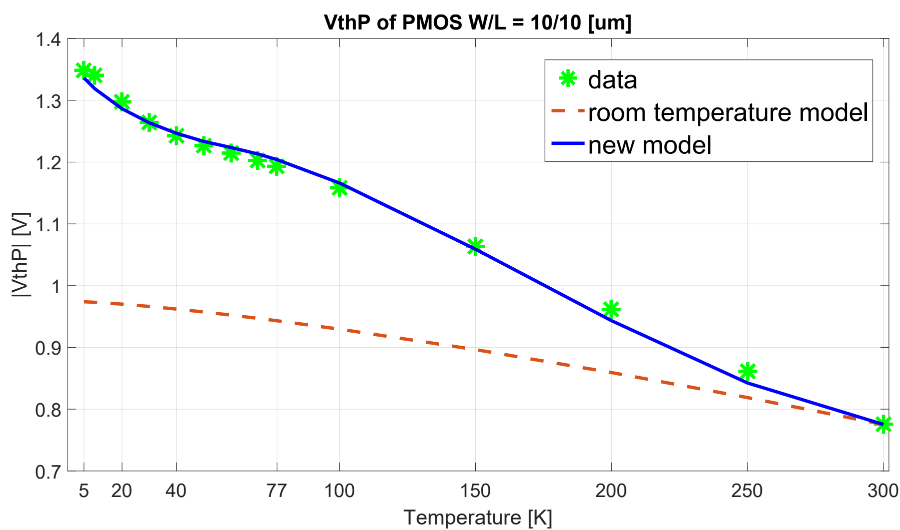


Figure 4.3: The temperature dependence of V_{T0} of PMOS: new model (Eq. (4.9)), conventional model (Eq. (4.1)) vs. experimental data (symbol)

The parameters η and β in the threshold voltage model for PMOS are 1.45 and 17.15, respectively. Unlike the NMOS, the threshold voltage of PMOS does not saturate with decreasing temperature, rather it increases below 50 K as demonstrated in Fig. 4.3. The reason for this phenomenon could be due to the donors in P-channel suffering strong freeze-out. Consequently, further field-assisted ionization is required, alternatively, or the activation potential ϕ_{AF} must be set greater at very low temperatures. To model this effect, the freeze-out coefficient m for PMOS (Eq. (4.11)) is chosen as 0.9 for temperature below 50 K and 1.0 for above 50 K.

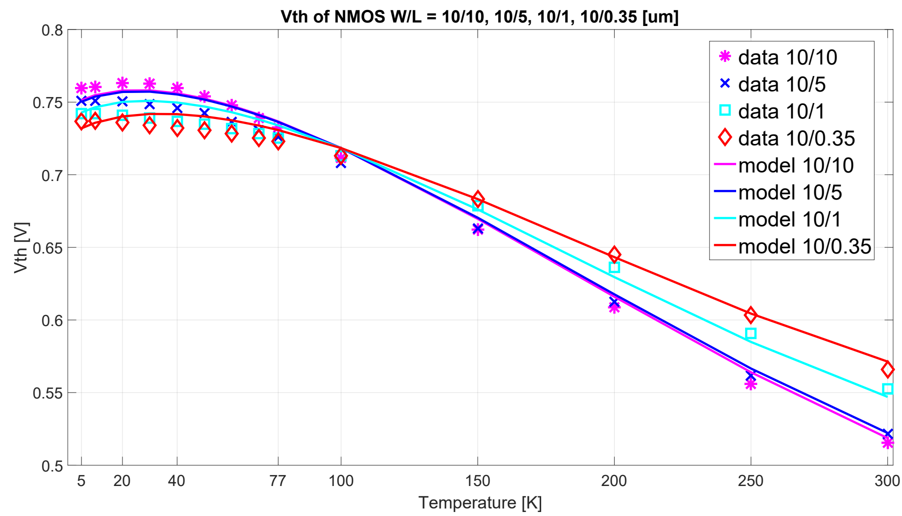


Figure 4.4: The short channel effects of NMOS V_T: model (–) vs. experimental data (symbol)

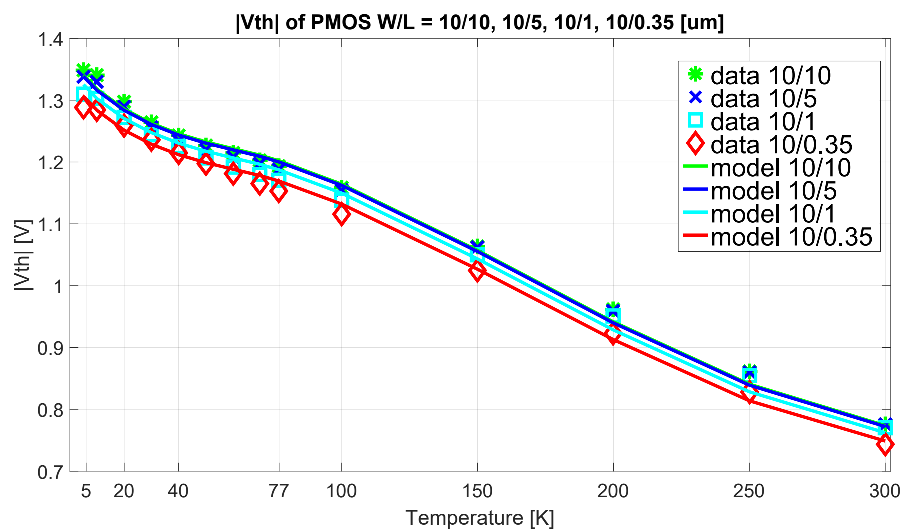


Figure 4.5: The short channel effects of PMOS V_T: model (–) vs. experimental data (symbol)

The V_T model of NMOS (δ_{VT} = 4.3) and PMOS (δ_{VT} = 0.075) with the short channel effects are depicted in Fig. 4.4 and Fig. 4.5, respectively. The data indicates that our equations model the temperature dependence of the threshold voltage for the long and short channel MOS over the 5–300 K temperature range. The maximum error between the proposed model and experiment is less than three percent.

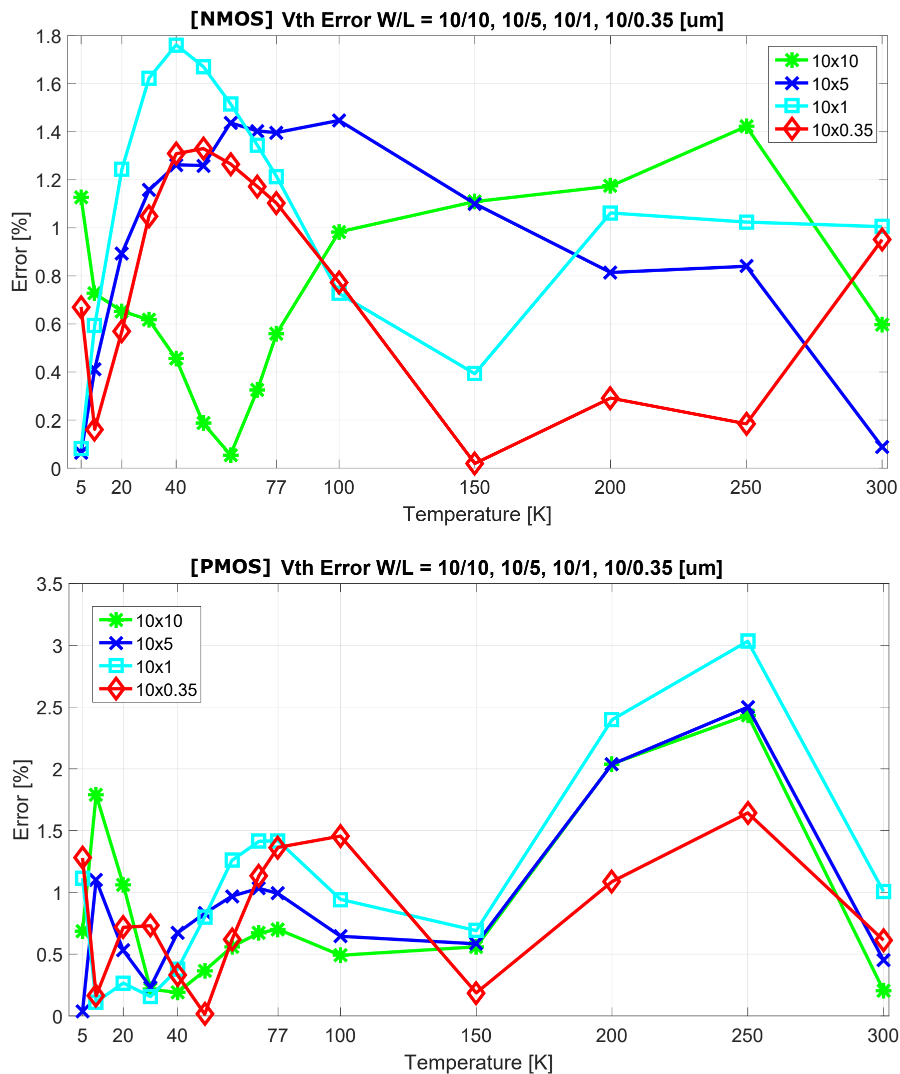


Figure 4.6: Errors between the proposed model and experimental data over the examined temperatures

4.6 Summary

This chapter has presented an enhanced threshold voltage model of NMOS and PMOS transistors for temperatures from 5 K to 300 K. The model is derived from the simplified Fermi potential which takes into account the carrier freeze-out effect. External field-assisted ionization is proposed and incorporated into the model to correct the threshold voltage. In addition, an empirical function that can be employed to estimate the short channel effects on the threshold voltage is also presented. The results from the proposed model demonstrate good agreement with data measured from fabricated chips. This model can also be adapted to fit with other technologies since it is derived from the physics of the bulk CMOS and process dependent parameters.

Chapter 5

DC model of MOSFETs for cryogenic circuit simulation

This chapter presents a semi-empirical MOS transistor model for circuit simulation over the 5-300 K temperature range. First, an introduction and a brief review of MOSFET models for low-temperature applications are presented. Next, an introduction of the proposed wide range temperature model of carrier mobility and series resistance is presented. Then, a compact current-voltage model, based on threshold voltage model, carrier mobility model and series resistance model, is presented along with its evaluation. Finally, discussion of the results and limitations of the model are provided.

5.1 Introduction

Circuit simulation is a vital step in integrated circuit (IC) design. Fabrication for an Application Specific Integrated Circuit (ASIC) is an expensive process, and hence, implementation of circuits have to be simulated and verified before it is sent to foundries. Simulation Program with Integrated Circuit Emphasis (SPICE) model is imperative for circuit simulation [18]. A good transistor model will help replicate device behaviour and provide a mean to validate designed circuits. Several transistor models have been introduced and some of them have become standard models in the semiconductor industry [110]. In particular, the Berkeley Short-channel IGFET (Insulated Gate Field Effect Transistor) Model or BSIM has been known as the most popular model used in CMOS IC design for the past decades. The BSIM models (BSIM3 and BSIM4) were developed based on the source-referenced threshold voltage-referenced models and several effects were implemented in the model through the threshold voltage and field-dependent mobility [23, 29]. Another standard model is the EKV model which was developed

based on an inversion-charge-based approach by experienced circuit designers and dedicated for analog and RF IC designs. Some other models derived from the surface potential-based MOSFET model such as PSP model [36] and HiSIM model [37] have been introduced and become more favourable in circuit simulations for deep sub-micrometer and nanometer technologies. Those standard models are widely used in commercial simulation tools such as Cadence Spectre, however, they are only used for devices operating at room temperatures (-40°C to 180°C) and none of them can be used at deep cryogenic temperatures [18, 111].

The demand for deploying MOSFET transistors at very low temperatures in control/interface circuits for quantum devices has recently increased [8, 112, 113]. Unlike the room temperature model, model developed for low-temperature simulation have to consider effects of incomplete ionisation due to carrier freeze-out and strong impact of series resistance [9, 20, 41].

Because of non-existing standard MOSFET model for cryogenic temperatures, circuit designers have to employ room temperature models and adapt them for low-temperature applications [15, 27]. Some attempts have been made to create low-temperature MOS models by modifying room temperature parameters to address their behaviour at low temperatures [47, 54]. Other studies introduced wide temperature range SPICE models by adding a new sub-circuit to account for the cryogenic effects [16], or by modifying the BSIM parameters to obtain a 20–300 K model [18]. Models devised for a specific temperature may need to be characterised at that temperature, and might not provide insight into the device behaviour over a wide temperature range, whereas adding sub-circuits or modified BSIM models are complicated and difficult to use in hand calculation. In addition, to promote circuits to be located next to quantum bits operating at a few Kelvins [5], proper MOS models faithful at these temperatures are required.

The following sections present model of carrier mobility, series resistance, and a SPICE model of bulk CMOS drain current operating from 300 K down to 5 K. Our I-V model is derived from SPICE Level 3 [24].

5.2 Carrier mobility and series resistance model

In order to develop a low-temperature SPICE model for CMOS transistor, temperature dependencies of each key parameters are studied. The threshold voltage model is presented in Chapter 4. This section presents wide temperature models of carrier mobility and series resistance, extracted from the proposed approach in Chapter 3.

5.2.1 Carrier Mobility

Chapter 2 presented several studies which have investigated the physical mechanisms that govern carrier mobility, providing both theory and practical models from room temperature down to liquid helium temperature (4.2 K) [9, 57].

Although theoretical models can represent the physical effects, they are difficult to use in circuit simulation [9]. Practical models with fitting parameters can provide a suitable compromise for efficient circuit calculations. As shown in Eq. (2.30), a wide-temperature mobility model has been introduced. This semi-empirical model can fit carrier mobility from room temperature down to liquid helium temperature. A disadvantage of this model is it requires several iterations in extracting series resistance and channel resistance to obtain a precise value of n, scattering mechanism relations, at a single temperature [96]. This issue will be magnified when the model is used at several temperatures. In addition, the non-integer exponent n might become a computational burden. Therefore, for the sake of simplicity, n = 2 is fixed to make it as similar as the room temperature model [64], and the carrier mobility model in Eq. (2.30) can be simplified as

$$\mu = \frac{\mu_m}{1+\theta_1(V_{GS}-V_T)+\theta_2(V_{GS}-V_T)^2}$$

$$\text{Or,} \tag{5.1}$$

$$\mu = \frac{\mu_m}{1+\theta_1 V_{GST}+\theta_2 V_{GST}^2}.$$

Here, θ_1 and θ_2 are fitting parameters (the mobility attenuation coefficients) which account for the mobility decrease in V_{GST}.

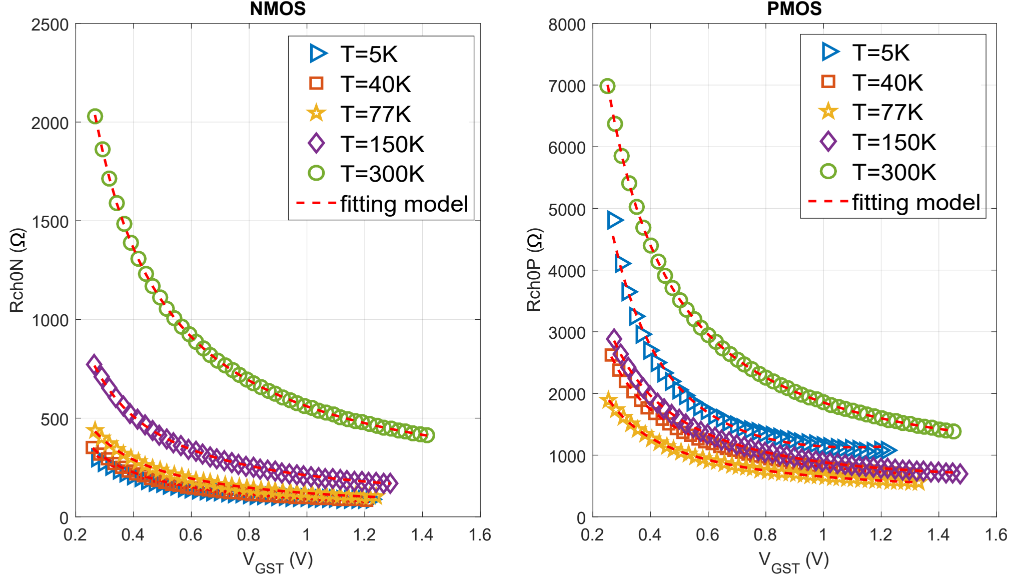


Figure 5.1: Fitting results of R_{ch0} at different temperatures

In Eq. (5.1), θ_1, θ_2, and μ_m are functions of temperature, and their values can be obtained from the best fit of the intrinsic channel resistance R_{ch0} (see Chapter 3). Figure 5.1 clearly shows that the fitting results of R_{ch0} are very close to the extracted data at all examined temperatures. These parameters, θ_1, θ_2, and μ_m, extracted from fitting model are shown in Table 5.1.

Table 5.1: Parameters of carrier mobility

Temperature (K)		5	20	40	77	100	200	300
NMOS	μ_m (cm^2/Vs)	2764	2895	2750	2185	1847	782	405
	θ_1 $(1/V)$	-0.143	-0.144	-0.133	-0.103	-0.090	-0.040	-0.022
	θ_2 $(1/V^2)$	0.337	0.340	0.314	0.243	0.211	0.095	0.051
PMOS	μ_g (cm^2/Vs)	188	234	307	401	369	203	125
	θ_1 $(1/V)$	-0.118	-0.141	-0.184	-0.246	-0.218	-0.117	-0.074
	θ_2 $(1/V^2)$	0.183	0.219	0.285	0.382	0.339	0.181	0.115

In order to represent temperature dependence of mobility in a compact SPICE model, polynomial fitting functions are used to model μ_m, θ_1, and θ_2 as shown in Eq. (5.2).

$$
\begin{aligned}
\mu_m &= {\mu_{m0}}^{U_{(T)}}, \\
\theta_1 &= \frac{\theta_{1,0}}{P_{(T)}}, \\
\theta_2 &= \frac{\theta_{2,0}}{P_{(T)}},
\end{aligned}
\tag{5.2}
$$

and,

$$U_{(T)} = u_0 + u_1\left(\frac{T}{300}\right) + u_2\left(\frac{T}{300}\right)^2 + u_3\left(\frac{T}{300}\right)^3 + u_4\left(\frac{T}{300}\right)^4,$$
$$P_{(T)} = p_0 + p_1\left(\frac{T}{300}\right) + p_2\left(\frac{T}{300}\right)^2 + p_3\left(\frac{T}{300}\right)^3, \tag{5.3}$$

where μ_{m0} is the maximum mobility at 300 K, $\theta_{1,0}$, $\theta_{2,0}$, u_i, p_i (i = 0:4) are fitting coefficients, while T is the temperature in Kevin. Table 5.2 shows the fitting coefficients in Eq. (5.2)

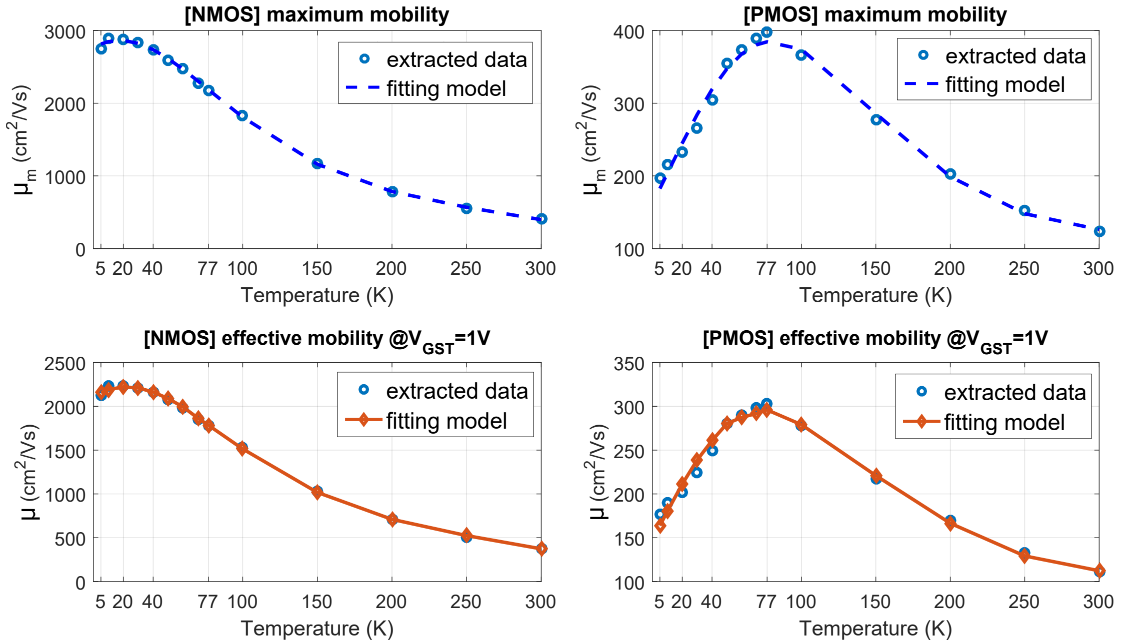


Figure 5.2: Fitting results of the carrier mobility at different temperatures

Substituting the fitting functions of Eq. (5.2) into Eq. 5.1, forms a temperature dependent model which can depict the carrier mobility effectively over the temperature range from 5 K to 300 K. Fitting results versus extracted data of the mobility at different temperatures are plotted in Figure 5.2. The goodness of fits (adjusted R-square) are 99.88% and 98.02% for NMOS and PMOS, respectively.

Table 5.2: Fitting coefficients used in Eq. (5.2)

		fitting coefficients
NMOS	μ_i	u_0 = 1.32; u_1 = 0.207; u_2 = -1.958; u_3 = 2.434; u_4 = -1.006
	$\theta_{1,0}$	-11.7
	$\theta_{2,0}$	27.7
	p_i	p_0 =79.68; p_1 = 7.51; p_2 = 466.6; p_3 = -11.46
PMOS	μ_i	u_0 = 1.055; u_1 = 1.547; u_2 = -4.161; u_3 = 3.588; u_4 = -1.026
	$\theta_{1,0}$	-132.1
	$\theta_{2,0}$	205
	p_i	p_0 = 1186; p_1 = -4830; p_2 = 1.062E4; p_3 = -5208

5.2.2 Source/Drain series resistance

In the sub-micrometer CMOS regime, the source/drain series resistance cannot be ignored due to the scaled channel length. In addition, as shown in Chapter 3, the series resistance is found impact device operation significantly when temperature decreases [20]. Therefore, its effect must be modelled.

The extracted source/drain series resistance of the short channel (L = 0.35 μm) can be empirically modelled using the first order polynomial function of overdrive gate voltage V_{GST} as follows

$$R_{sd} = R_0 + \frac{R_1}{V_{GST}}, \tag{5.4}$$

where R_i (i=0, 1) is the fitting function of temperature, and can be expressed as

$$R_i = r_0 + r_1 T + r_2 T^2 + r_3 T^3 + r_4 T^4. \tag{5.5}$$

In Equation (5.5), the fitting coefficients r_m (m = 0:4) is listed in Table 5.3:

Table 5.3: fitting coefficients used in Eq. (5.5)

fitting coefficients		r_0	r_1	r_2	r_3	r_4
NMOS	R_0	118	-0.0516	-0.0013	-5.326E-7	1.203E-8
	R_1	74.63	-0.5393	7.296E-4	1.054E-5	-3.093E-8
PMOS	R_0	2327	-38.03	0.2937	-1.074E-3	1.46E-6
	R_1	6344	-153	1.329	-4.79E-3	6.123E-6

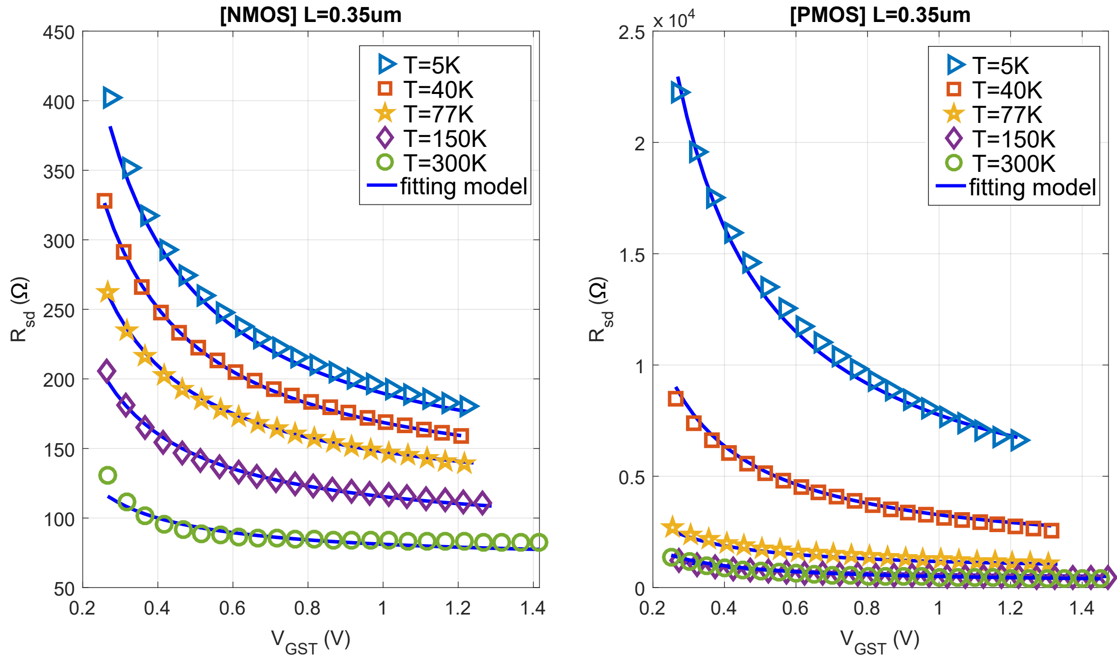


Figure 5.3: Fitting results of the series resistance at different temperatures

Substituting R_0 and R_1 in Eq. (5.4), the equation is now able to express the series resistance of the NMOS and PMOS from 5 K to 300 K. Fitting results are shown in Figure 5.3.

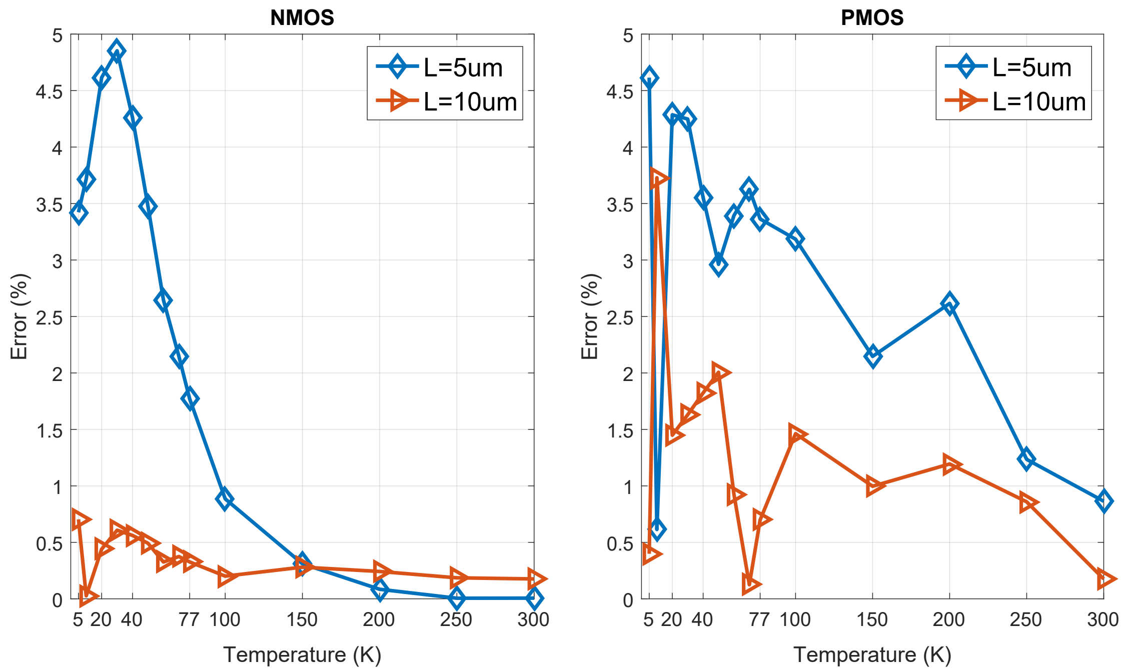


Figure 5.4: Errors when short channel R_{sd}, Eq. (5.4), is used for long channel transistors.

Since the series resistance varies with channel lengths as mentioned in Chapter 3, fitting coefficients have to be changed for different transistors. However, variations of series resistance due to variations of channel lengths are small compared to the total series resistance ($R_{sdL} \ll R_{sd}$) when $V_{GS} \gg V_T$ (strong inversion region). Moreover, the series resistance has less impact on longer channel devices, thus, the formula for the short channel, Eq. (5.4), can be used for long channel transistors. The maximum difference is less than 5% when using Eq. (5.4) for long channel devices at all temperatures (Figure 5.4).

5.3 I-V characteristics

This section presents the new I-V model derived the strong inversion I-V model SPICE level 3. The threshold voltage model, the mobility model and impact of series resistance are incorporated into a compact model which is described in the Verilog-A language. The model can then be used in a standard IC simulation tool (Cadence Spectre) and used to simulate MOSFET devices from room temperature down to 5 K.

As shown in Chapter 2, drain current of transistors operating in strong inversion regime can be described using Eq. (2.13) and Eq. (2.14) for linear region and saturation region, respectively.

In order to create a compact I-V model for both linear and saturation regions, rather than having an abrupt transition at V_{DS} = V_{DSAT}, an effective Drain-Source voltage $V_{DS,eff}$ is introduced [24, 46],

$$\begin{aligned} V_{DS,eff} &= V_{DSAT} - 0.5\left[V_d' + \sqrt{V_d'^2 + 4\delta_{DS}V_{DSAT}}\right] \\ V_d' &= V_{DSAT} - (V_{DS} - V_{Td}) - \delta_{DS}, \end{aligned} \tag{5.6}$$

where δ_{DS} is the smooth parameter, and V_{Td} is the drain threshold voltage (see Chapter 2, section 2.3.4) corresponding to the impact of series resistance. V_{Td} is computed as V_{Td} = $I_D R_{sd}/2$, where I_D is the drain current in linear region, Eq. (2.13).

Replacing V_{DS} in Eq. (2.13) and V_{DSAT} in Eq. (2.14) by $V_{DS,eff}$, the I-V model now becomes

$$I_D = \mu C_{ox}\frac{W}{L}\left(V_{GST} - \frac{(1+F_B)}{2}V_{DS,eff}\right)V_{DS,eff}\frac{1}{1+T0}\ . \tag{5.7}$$

In Eq. (5.7), μ is the effective mobility described in Eq. (5.1), while V_{GST} = V_{GS} - V_T, with V_T is the threshold voltage in Eq. (4.13). This formula can express the drain current of MOS transistor operates in both linear and saturation regions.

In MOS3 model, due to its simplicity, the model exhibits several derivative discontinuities

in short channel calculations, which leads to slow down simulation speed [32]. To overcome this issue, in the new model, instead using Eq. (2.15) in calculating geometry effects F_B, geometry effects are calculated using the BSIM model. F_B is determined as below

$$\begin{aligned} F_B &= \frac{\gamma F_S}{4\sqrt{2\phi_F - V_{BS}}} + F_N, \\ F_N &= \frac{\delta_W \pi \varepsilon_{Si}}{2C_{ox}W}, \\ F_S &= 1 - \frac{\Delta V_{TH}}{V_{TH}}, \end{aligned} \tag{5.8}$$

where ΔV_{TH} represents the geometries effects as shown in Eq. (2.21).

By combining temperature dependent models of threshold voltage, mobility and series resistance which take into account cryogenic effects, our compact I-V model is able to replicate the current at very low temperatures.

5.4 Model validation

5.4.1 Model implementation

A SPICE model now can be implemented based on Equation (5.7) which express the drain current formula in linear and saturation regions of operation for bulk CMOS. To implement the proposed model, the analog device behavioral language Verilog-A [114, 115] is used which allows more physics-based compact models to be developed [18]. Other advantages when using the Verilog-A are its computation speed and compatibility [116], make it easy to import to a standard simulator, i.e Cadence Spectre.

Figure 5.5 shows a screenshot of Verilog-A code and parameter setup. A full description of the Verilog-A model is provided in Appendix C. Our model can successfully import and simulate devices in Virtuoso Analog Design Environment (Cadence Virtuoso ADE) as shown in Figure 5.6. The model uses only a single set of parameters, which is based on room temperature BSIM parameters for standard simulation tools, to predict the I-V characteristics at all temperatures.

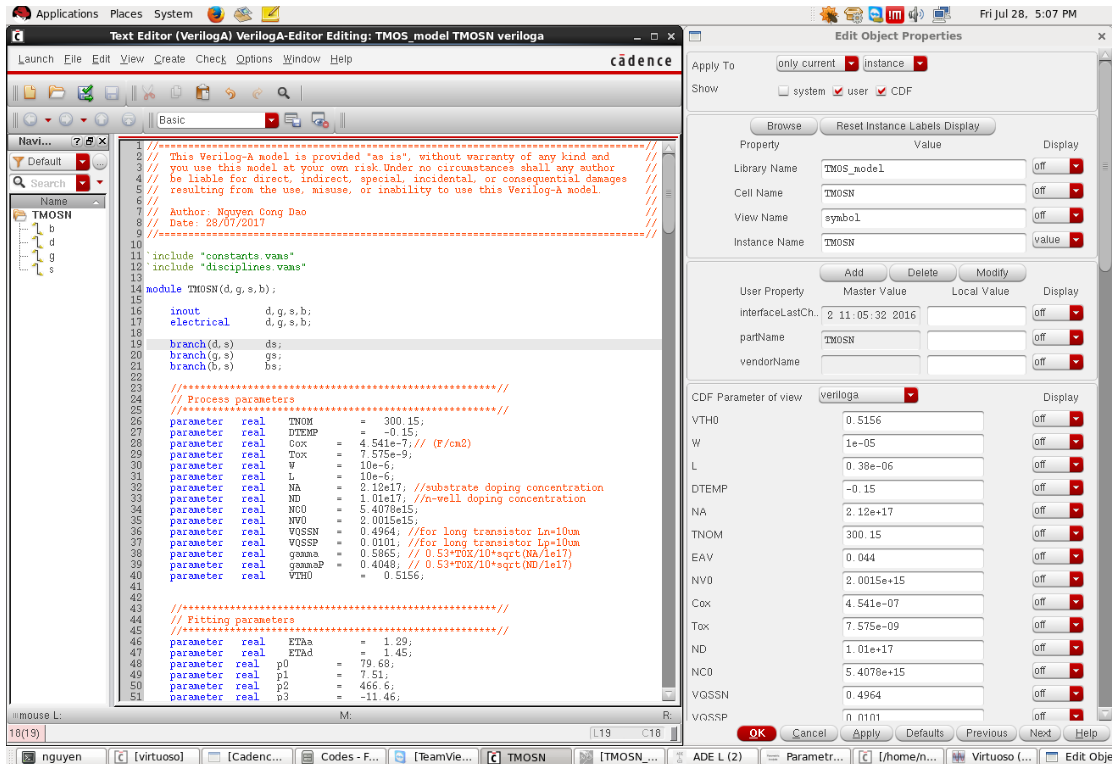


Figure 5.5: A screenshot of Verilog-A code and parameter setup

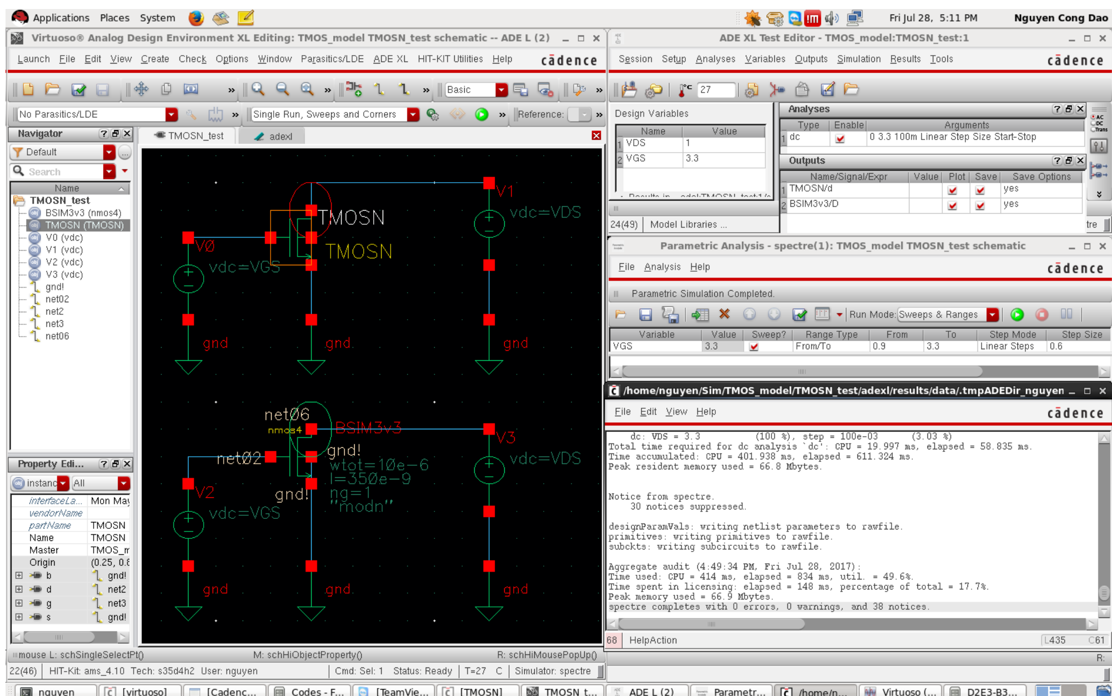


Figure 5.6: Simulation setup in Virtuoso Analog Design Environment

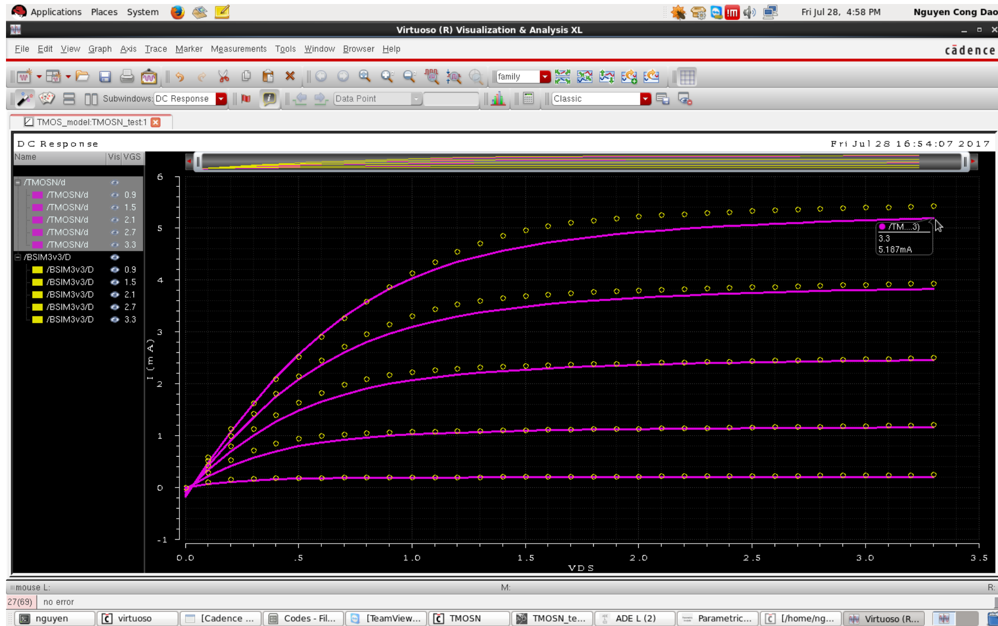


Figure 5.7: Simulation result from the new model (solid lines) and the BSIMv3.3 model (circles)

A comparison of simulation results at 300 K from the new model and the BSIM model, a built-in model in Cadence Virtuoso ADE, is illustrated in Figure 5.7. It clearly shows that the new model obtains similar results as the BSIM model (version 3.3) at room temperatures.

5.4.2 Results and Discussion

Experimental data is used to validate the new model over a wide range of temperature. Results from the model are plotted against measured currents different temperatures in Figure 5.8 and 5.9 for NMOS and PMOS, respectively. The model can provide a good approximation of the drain current in the strong inversion regime from 5 K to 300 K. In particular, the fidelity of the model at $V_{GS} \gg V_T$, i.e. V_{GS} = 3.3 V, is about 95% compared to measured data. Figure 5.8 and 5.9 depict comparisons of the model versus experimental data at different temperatures. It shows that the accuracy of the model decreases when transistor operating below 40 K in weak inversion regime. It is because the proposed extraction approach was for strong inversion operation, resulting in imprecise values of the maximum carrier mobility and velocity saturation. This limitation could be solved if the current parameter set is replaced by a new one obtained from a better extraction approach.

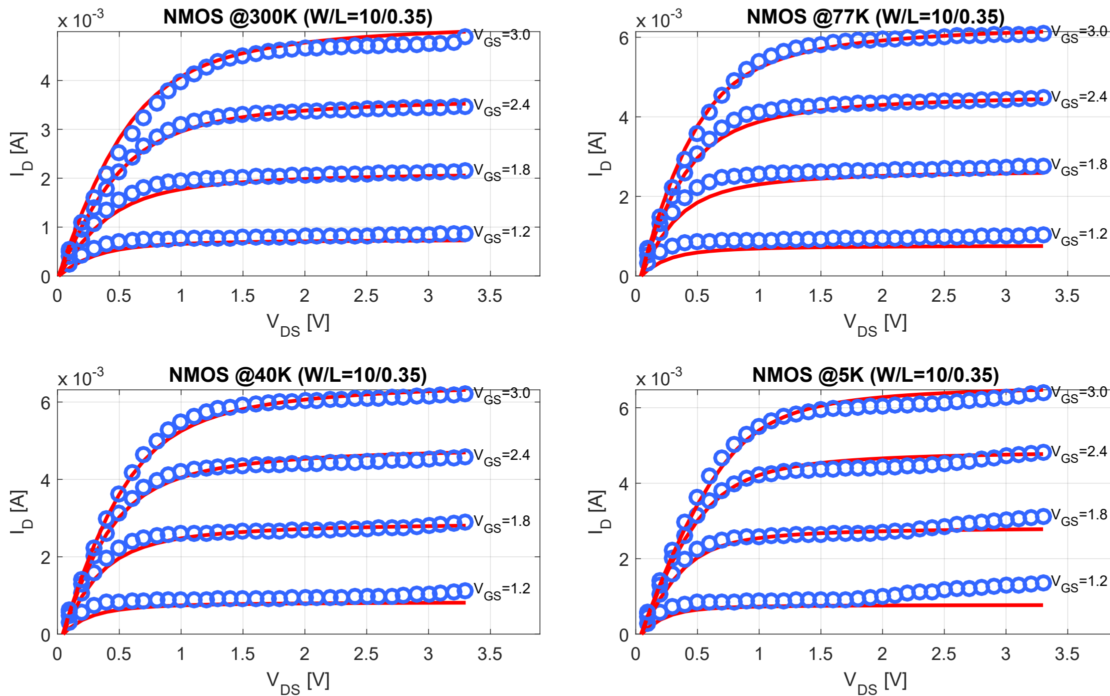


Figure 5.8: I_D-V_{DS} characteristic of NMOS at different temperatures: the model (–) vs. experimental data (o).

Other effects that may impact the model accuracy are kink effect and hysteresis phenomenon. As mentioned, these phenomena only affect device characteristic at very low temperatures, T < 30 K, as shown in the current of the NMOS at 5K (Figure 5.8). Because they do not occur in both types of transistors, and their impact is not significant over a wide temperature range in the examined technology (AMS C35, S35) or other similar submicrometer technologies (0.25 μm [54], 0.35 μm [27]), these effects are ignored in the proposed model.

It is worth noting that the drain threshold voltage V_{Td} has been implemented to show the impact of series resistance at all temperatures. This helps improve accuracy when devices operate in the linear region, especially at very low temperatures. It can distinguish that $V_{Td} > 0$ which means V_{DS} need to be greater than V_{Td} to active the drain current. The model well fit to the measured current as shown in Figure 5.8 and 5.9.

Comparison of the model and measured current in the linear region (V_{DS} = 0.1V) at all temperatures is shown in Figure 5.12. The results depict good agreement between the model and the measured data over the entire temperature range.

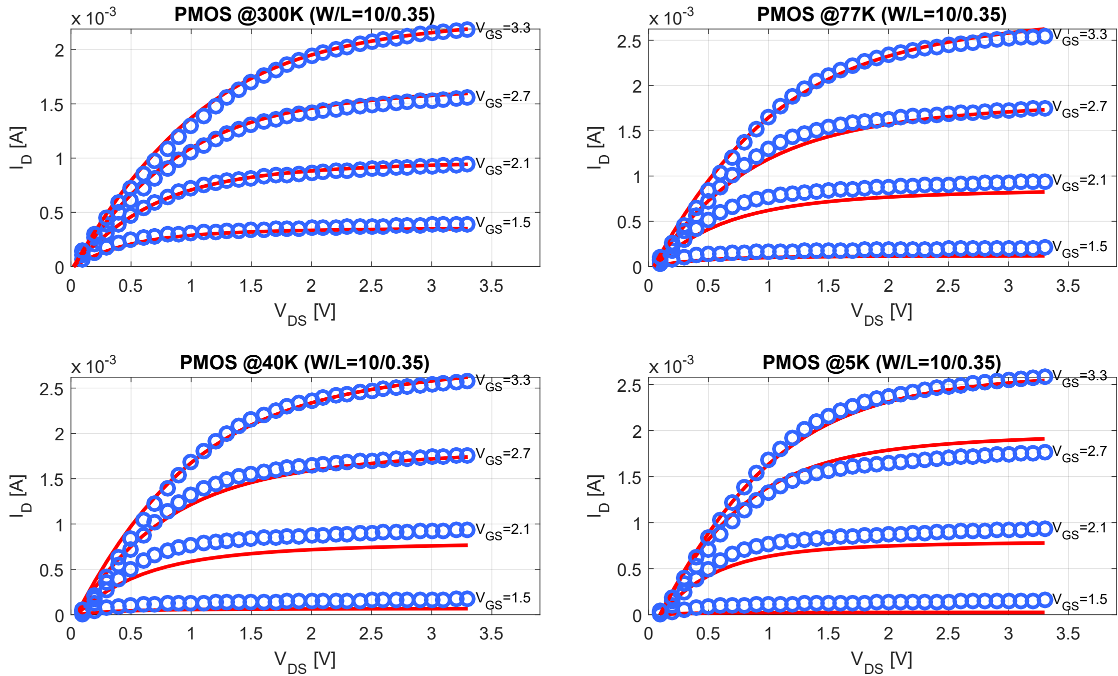


Figure 5.9: I_D-V_{DS} characteristic of PMOS at different temperatures: the model (–) vs. experimental data (o).

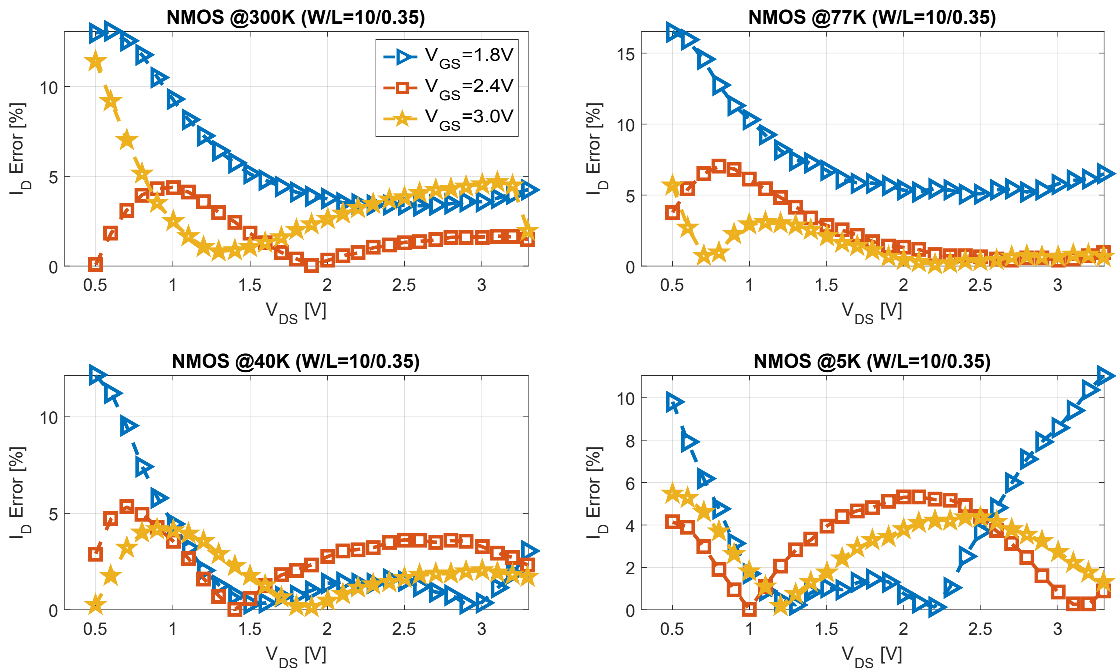


Figure 5.10: Error between the model and measured data of NMOS current versus V_{DS}

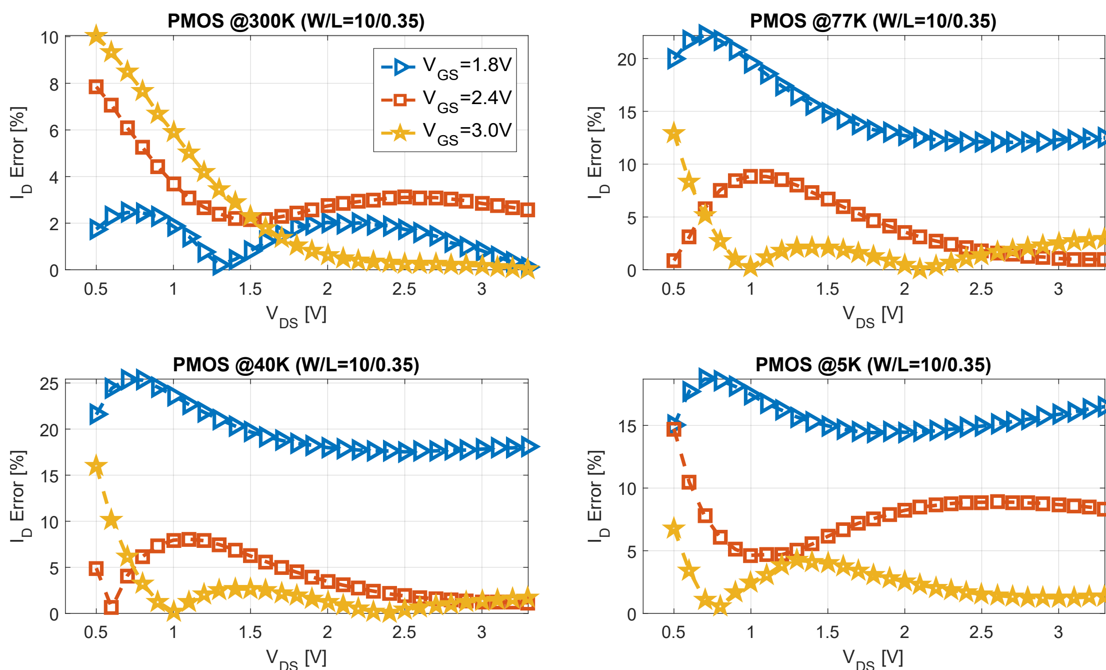


Figure 5.11: Error between the model and measured data of PMOS current versus V_{DS}

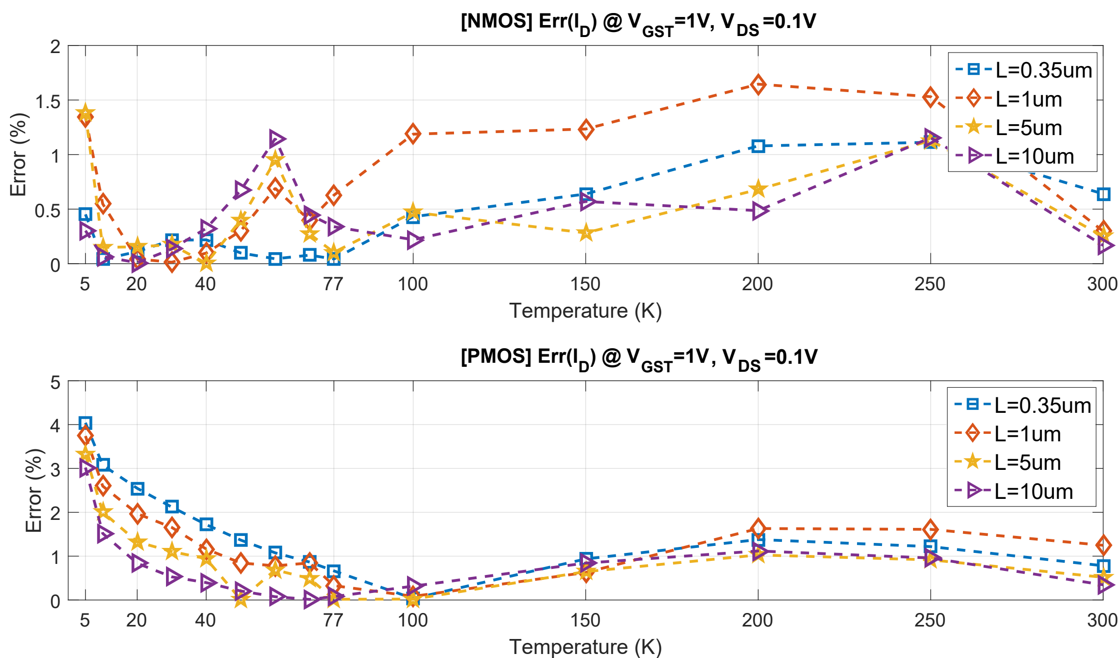


Figure 5.12: Error between the model and measured data of NMOS, PMOS current at all examined temperatures

5.5 Summary

A SPICE model of bulk MOSFETs for circuit simulation from room temperature down to 5 K has been presented. The enhanced threshold voltage model, a wide temperature model of mobility, and the impact of series resistance are incorporated into a semi-empirical compact model to express the drain current in both linear and saturation regions. The model was successfully described in the Verilog-A language and simulated in a standard design environment (Cadence Virtuoso ADE). Results indicate that the model can replicate the I-V characteristics of the MOS transistor at all examined temperatures. It is the first compact model which has the capability to simulate bulk MOSFETs at near liquid helium temperature.

Chapter 6

Matching properties of MOSFETs

This chapter studies matching properties of MOSFETs over the 5-300 K temperature range. First, an overview of MOSFET matching at low temperatures is presented. Then, the next section presents experimental setup, test chips and measurements from which matching properties of MOS transistor in a wide range of temperature are examined. Next, the proposed formula to calculate variations of the drain currents along with comparison results between the proposed formula and conventional models is introduced. Effect of device dimensions on parameter mismatch at low temperatures is also discussed in the next section. The chapter is summarised in the last section.

Results from this chapter were partly reported and published in [20].

6.1 Introduction

Device matching is an important property for analog CMOS circuit design. It refers to differences in characteristics among nominally identical transistors operating under the same condition. Parameter variations of MOS transistors, causing drain current mismatch is one of the main issues that limit the performance of analog circuits. For example, a few millivoltage difference in the threshold voltage might strongly impact the effective number of bit of an analog-digital converter (ADC), degrading performance [86]. Matching of MOSFETs has been extensively studied at room temperature [87, 117, 118], but it has not been deeply investigated over a wide range of temperature, and especially at very low temperatures.

It has been shown that CMOS devices at low temperatures have several advantages such as faster speed and circuit performance, however, device matching degraded at cryogenic temperatures due to incomplete ionisation and enhanced quantum effect [40, 72].

Previous works in cryogenic CMOS design showed that matching of current mirrors degrades when operated at 4.2 K compared to the matching at room temperature [119]. A brief review in [17] reported matching properties of 0.18 μm CMOS at 77 K. It reported that variations of MOS parameters such as threshold voltage (V_T), current factor (β) and body effect factor (γ) are either constant or increase at cryogenic temperatures, depending on the type of transistor. In particular, increases in variations of the threshold voltage, the current factor of NMOS at 77 K were about 1.25 and 2.5 times greater compared to the values at 300 K. Variation of the PMOS threshold voltage was shown as a constant while the current factor variation of PMOS slightly varied with decreasing temperature. This work also reported increases in variations of drain currents at 77 K. It concluded that the cause of the device mismatch is mainly due to freeze-out of carriers at cold temperatures. Similar results were obtained in [40] when the authors examined a 90 nm bulk nMOSFETs operating at cold temperatures. For example, the threshold voltage fluctuation of NMOS W/L = 0.48/0.08 [μm] increased consistently from 23 mV at 300 K to 48 mV at 40 K. Another work presented a comparison of matching properties of Fully-Depleted Silicon on Sapphire (FD-SOS) CMOS at liquid helium temperature and room temperature [120]. This work also observed that variations of the threshold voltage, current factor, and drain current increased proportionally with device geometries when transistors operating at 4.2 K.

Although dependence of device matching on temperature has been well observed, a proper model to estimate variations of MOS transistor parameters and its current at deep cryogenic temperatures (below 40 K) has not been reported. In next sections, for the first time, variations of bulk CMOS parameters and matching of the drain current from room temperature down to 5 K are shown. A new formula for the current mismatch based on MOSFET parameters and series resistance is then introduced. The proposed model more accurately predicts the mismatch of current over the entire examined temperatures.

6.2 Experimental setup and parameter extractions

This section presents the test circuits, setup of the experiment, and measurements from which matching properties of MOS transistors are studied.

6.2.1 Test circuits and experimental setup

The MOS transistors used in this study were fabricated in the Austrian MicroSystems 0.35 μm CMOS (C35) p-substrate mixed signal process. Two test chips were fabricated: the QNL2 CMOS consisting of 64x64 NMOS transistors (Fig. 6.1), and the Mulberry consisting of PMOS

and NMOS, each type has 32x32 transistors (Fig. 6.2).

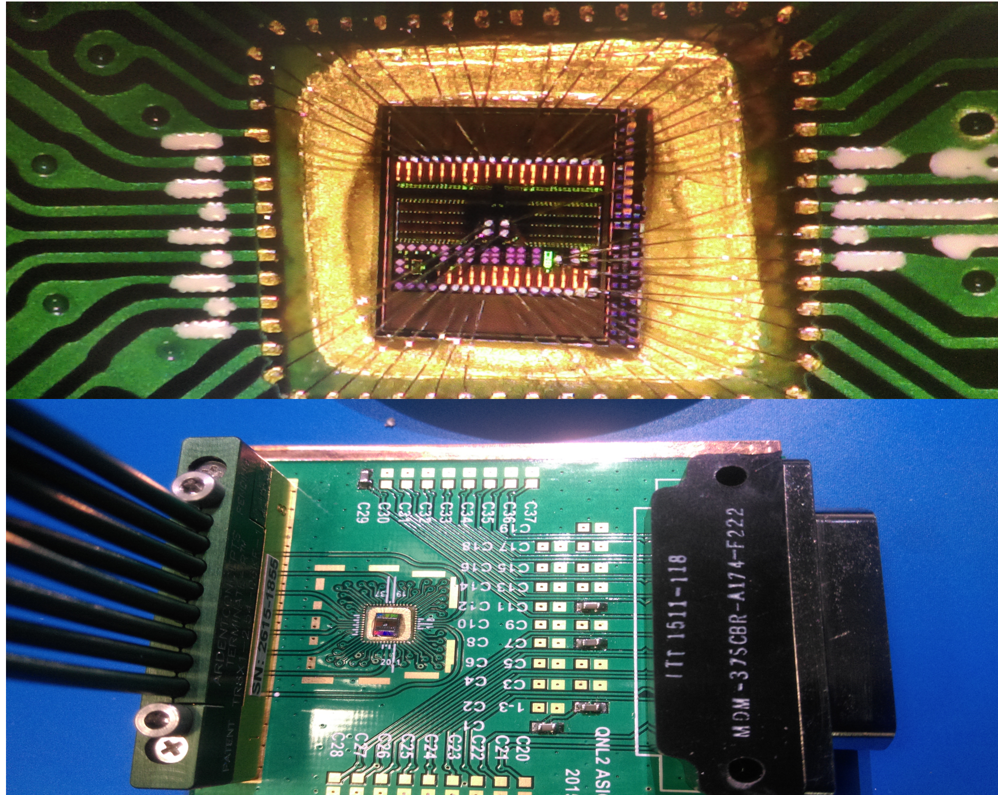


Figure 6.1: Bonded chip (QNL2 CMOS) and test PCB.

PMOS, NMOS transistors were placed in arrays including several same-size transistor blocks. Each block has 16 transistor with the device size ranging from W = 0.4, 1, 5, 10 μm and L = 0.35, 1, 5, 10 μm. W and L covered from minimum technology feature up to long and wide channel devices (10x10 μm^2).

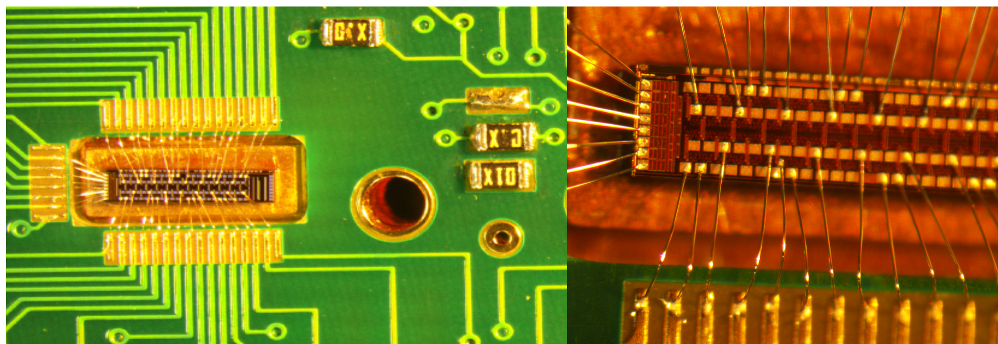
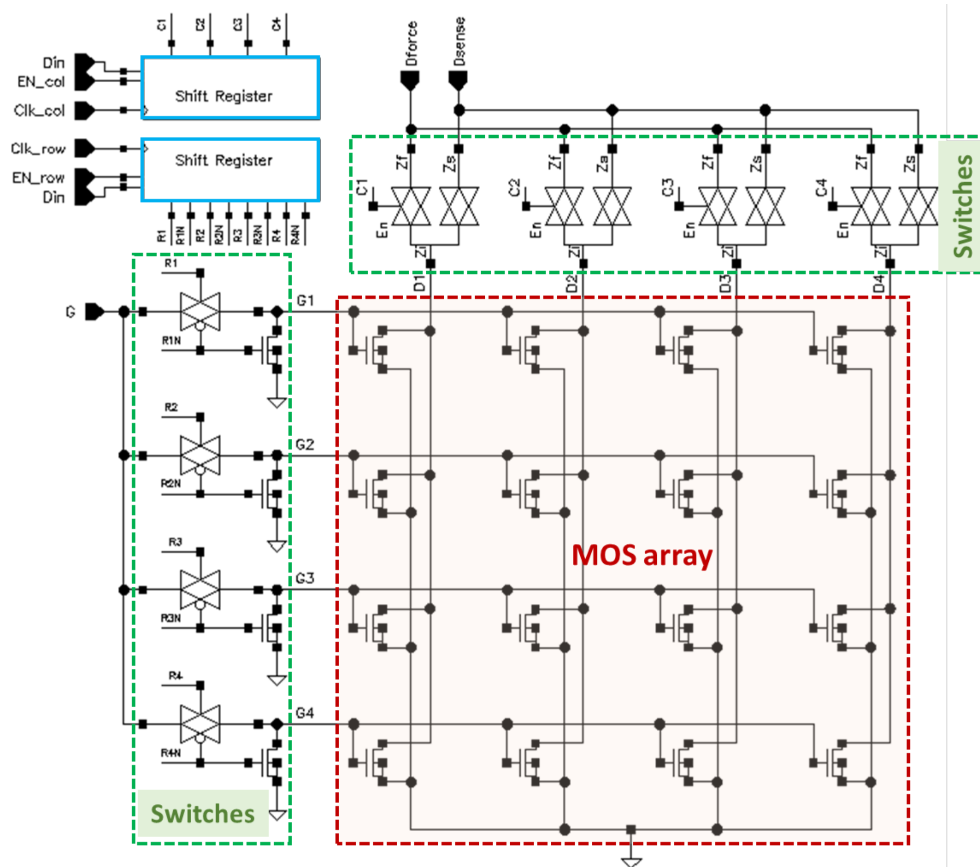


Figure 6.2: Bonded chip (Mulberry) and test PCB.



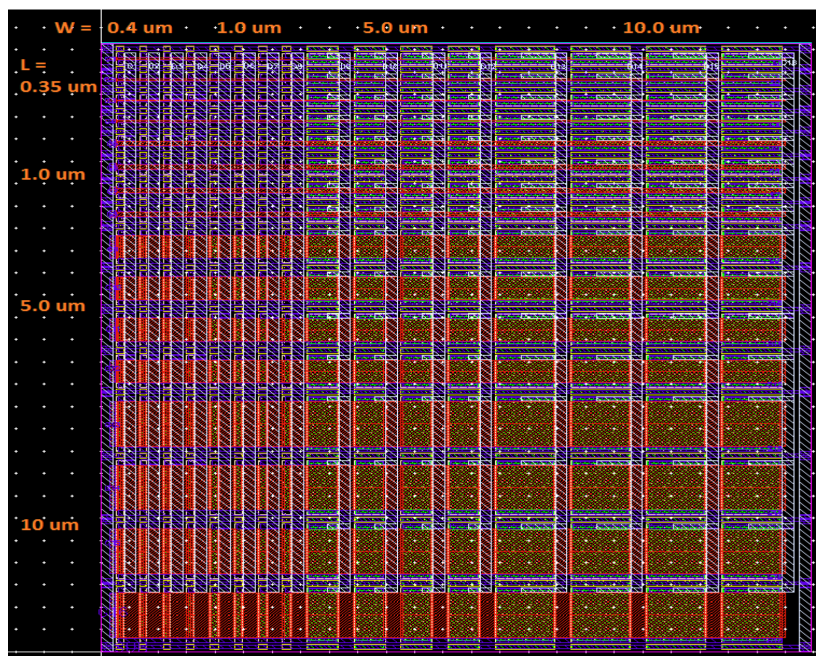


Figure 6.3: A circuit diagram of the test circuit illustrated for a 4x4 array (top) and layout of an MOS array (16x16 transistors).

A circuit diagram and an array layout are illustrated in Figure 6.3. Transistors used a common gate for each row and common drains for columns in the array. The source and substrate (bulk) terminals were all connected to GND for NMOS and to VDD for PMOS. Separated Force and Sense pads (Fig. 6.3) were used to eliminate effects of transmission gates, i.e. voltage drop, and parasitic resistance of cables [121]. Two shift registers were implemented to address rows (Gates) and columns (Drains) of transistors. This addressing method can select a single transistor in the array and all the characterisation of transistors in all operating regions.

6.2.2 Experimental setup

The test chips were mounted in a Closed Cycle Refrigerator-based (CCR) cryogenic probe station (LakeShore CRX-4K) fitted with temperature controllers (LakeShore TC336) to test MOS transistors in a wide range of temperature from 300 K down to 10 K. Because of self-heating, devices measured in the probe station at very low temperatures (below 10 K) might not exactly reflect the device temperature. Therefore, a dilution refrigerator (Leiden Cryogenics CF450) was used in measurements to obtain a stable temperature. The temperature recorded by thermometers (Cerium Magnesium Nitrate - CMN) at the sample plate was about 5 K.

A Matlab program was developed to control temperature (LakeShore TC336), and generate waveforms from an arbitrary waveform generator (Tektronix 5014 AWG) to select devices from the array. It also controlled a semiconductor analyzer (Keysight B1500A) to conduct measurements and store results. Figure 6.4 is a photograph showing electronic equipments used in the experiment.

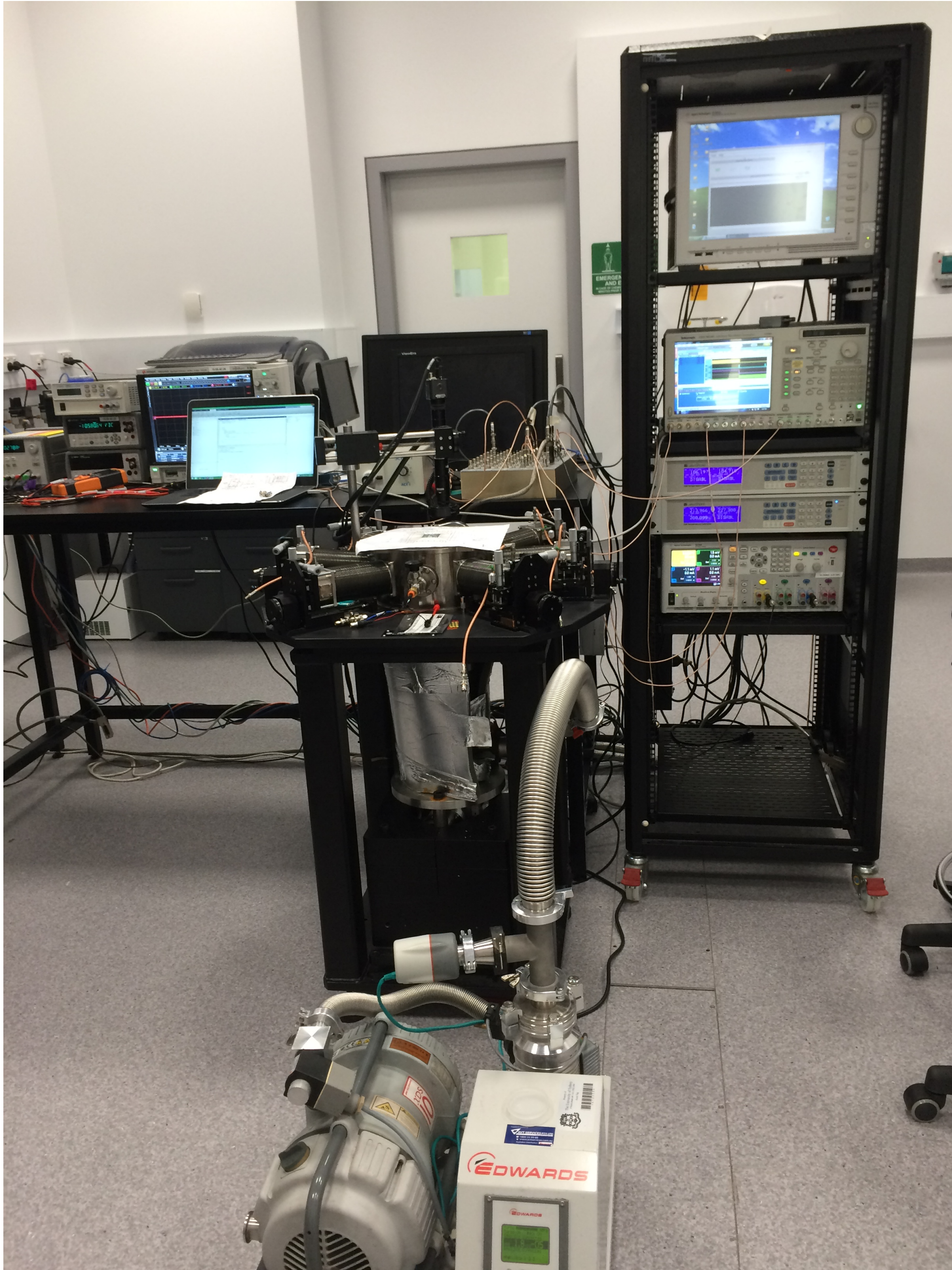


Figure 6.4: Photograph showing electronic equipment used in the experiments

6.2.3 Measurements and parameter extractions

Current-voltage (I_D - V_{GS} and I_D - V_{DS}) measurements from each single transistor were performed. Pulse measurement method with duty cycle 10% out of 5 ms was applied to minimise the self-heating effect. Errors from measurements can be neglected as because variations when

repeating measurements σ_{err} is much less than parameter variations σ_{var}. For example, the variation of the drain current of NMOS W/L = 1/1 [μm] at V_{GS} = 2.7 V, V_{DS} = 3 V is σ_{I_D} = 1.419 μA while σ_{err} = 0.088 μA. In this study, due to being limited to a small number of test chips, the process mismatch (parameter variation among different chips, different wafers) was not examined. This work only investigated mismatch of transistors on the same chip (same die).

The approach used to obtain transistor parameters: threshold voltage, mobility, and series resistance have been presented in Chapter 3 and 4. Extracted values of these parameters were used to calculate their mismatch. Parameter mismatches were examined globally among transistor array and locally between two adjacent transistors. The minimum distance between two adjacent transistors is about 2μm, whereas the maximum distance between two same size transistors is about 300 μm. For each transistor size, 96 pairs were used to study of pair current mismatch.

6.3 Drain current matching

6.3.1 Matching model

Drain current variability is one of the critical problems in scaled MOSFETs. It has been extensively studied and it is well known that threshold voltage and current gain factor fluctuations are the major sources of drain current mismatch [87]. As device channel length is scaled down, source/drain series resistance becomes non-negligible in the total device resistance [92]. For short channel devices, R_{sd} fluctuations are an additional contributor to the drain current variability [91, 122]. Therefore, R_{sd} have to be involved in a reliable drain current variability model as shown in Eq. (2.40). In this model, correlations between V_T, μ, while R_{sd} fluctuations are considered negligible as R_{sd} is assumed constant.

The conventional models (Eq. (2.39) and Eq. (2.40)) are widely used and accurate for devices operating in the strong inversion region at room temperature [91]. However, for a wide range of temperatures, since the channel resistance, R_{ch}, and series resistance vary significantly with the gate voltage and temperature, the correlation between series resistance and channel resistance must be taken into account. Based on the current model $I_D = V_{DS}/(R_{ch} + R_{sd})$, the current variation, from a first order Taylor approximation, can be obtained as

$$
\begin{aligned}
\sigma^2_{\left(\frac{\Delta I_D}{I_D}\right)} &= \left(\frac{1}{I_D}\frac{\partial I_D}{\partial R_{ch}}\right)^2 \sigma^2_{\Delta R_{ch}} + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial R_{sd}}\right)^2 \sigma^2_{\Delta R_{sd}} \\
&\quad + 2\frac{1}{I_D^2}\frac{\partial I_D}{\partial R_{ch}}\frac{\partial I_D}{\partial R_{sd}}\rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}} \\
&= G_d^2\left(\sigma^2_{\Delta R_{ch}} + \sigma^2_{\Delta R_{sd}} + 2\rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}}\right),
\end{aligned}
\tag{6.1}
$$

where $\rho_{(\Delta R_{ch},\Delta R_{sd})}$ is the correlation between R_{ch} and R_{sd}, $\sigma_{\Delta R_{ch}}$ and $\sigma_{\Delta R_{sd}}$ are variations of channel resistance and series resistance, respectively.

The variability $\sigma_{\Delta R_{ch}}$ can be derived from threshold voltage variations, $\sigma_{\Delta V_T}$, and mobility variations, $\sigma_{\Delta\mu/\mu}$, as follows

$$
\begin{aligned}
\sigma^2_{\Delta R_{ch}} &= \left(\frac{\partial R_{ch}}{\partial \mu}\right)^2 \sigma^2_{\Delta\mu} + \left(\frac{\partial R_{ch}}{\partial V_T}\right)^2 \sigma^2_{\Delta V_T} \\
&= \frac{1}{G_d^2}\left((1-G_dR_{sd})^2\sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{V_{th}}\right).
\end{aligned}
\tag{6.2}
$$

It is worth noting that the correlation between μ and V_T can be negligible. Substituting $\sigma^2_{\Delta R_{ch}}$ in Eq. (6.1) by (6.2), the current matching model becomes

$$
\begin{aligned}
\sigma^2_{\left(\frac{\Delta I_D}{I_D}\right)} &= (1-G_dR_{sd})^2\sigma^2_{\frac{\Delta\mu}{\mu}} + \left(\frac{g_m}{I_D}\right)^2 \sigma^2_{V_T} \\
&\quad + G_d^2\sigma^2_{\Delta R_{sd}} + 2G_d^2\rho_{(\Delta R_{ch},\Delta R_{sd})}\sigma_{\Delta R_{ch}}\sigma_{\Delta R_{sd}}.
\end{aligned}
\tag{6.3}
$$

This expression estimates variations of the drain currents from variations of transistor parameters and the correlation between series resistance and channel resistance.

6.3.2 Model validation

Validation of the proposed mismatch model, Eq. (6.3), now will be presented in this section. Note that all variations of parameters, channel resistance and series resistance are calculated from their extracted values which obtained from 96 adjacent pairs in the transistor array.

Current variations of NMOS and PMOS, calculated from the model, are plotted against measured data in Figure 6.5 and 6.6. These figures also show matching results obtained from the conventional matching formula (Eq. (2.40)).

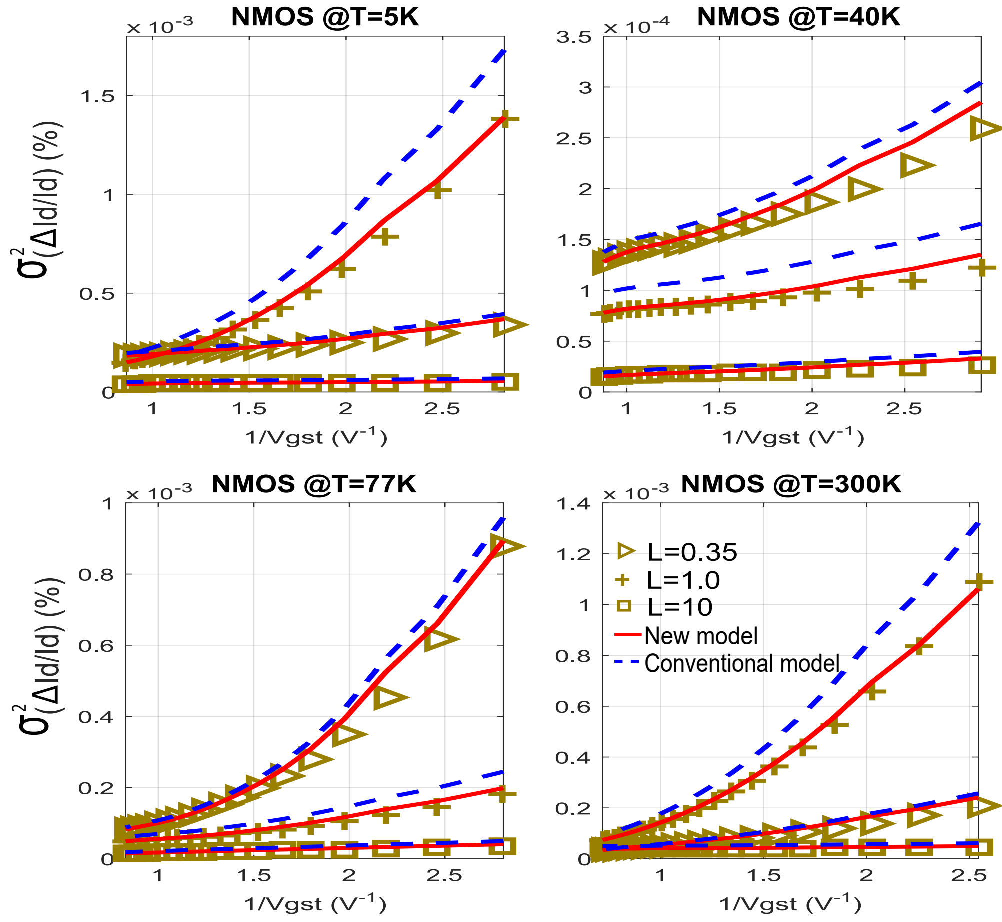


Figure 6.5: Current variations of NMOS with W=10μm, L=10, 1, 0.35μm: data (symbol) vs. proposed model (solid line) and conventional model (dash line)

It clearly shows that the model (red lines) fit well to experimental data compared to the existing model (dashed blue lines) at all examined temperatures. In particular, at 300 K, the proposed model and the existing model have similar results in strong inversion (V_{GST} = 1V) for both PMOS and NMOS devices. However, the accuracy of the existing model declines at low temperatures, especially for short channel devices. Taking into account the correlation between channel resistance and series resistance helps the model fit to the experimental data from 300 K down to 5 K. Errors between the proposed model, the conventional model versus measured data are depicted in Fig. 6.7 and Fig. 6.8. Table 6.1 shows comparisons between the model and the existing model for short channel devices.

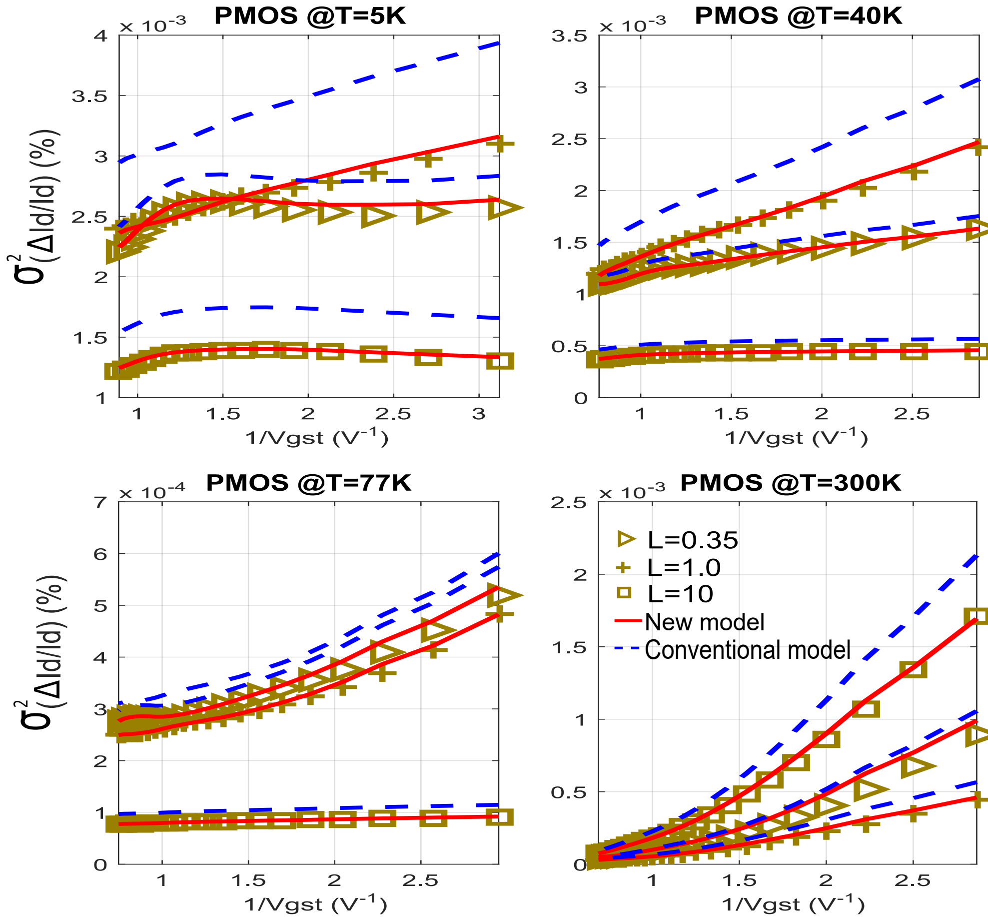


Figure 6.6: Current variations of PMOS with W=10μm, L=10, 1, 0.35μm: data (symbol) vs. proposed model (solid line) and conventional model (dash line)

Table 6.2 provides detailed variations of each dominant parameter considered in the current mismatch. In this table, variations of the threshold voltage, mobility, series resistance and the current of both long, short transistors at V_{GST} = 1 V are given. It can be seen that most of the parameter factors increase as temperature decreases, i.e. current matching degrades at low temperatures. Noting that the current magnitude increases with decreasing temperature mainly due to increase in carrier mobility and a decrease in channel resistance. Normalised current variations over the studied temperatures are shown in Figure 6.9. In general, the current variations in both PMOS and NMOS transistors change slightly from 300 K down to 100 K and then increase more dramatically as temperature further decreases. An explanation for this increased variation at cryogenic temperatures is due to the freeze-out of carriers which strongly impacts on the effective dopant concentrations and the carrier mobility.

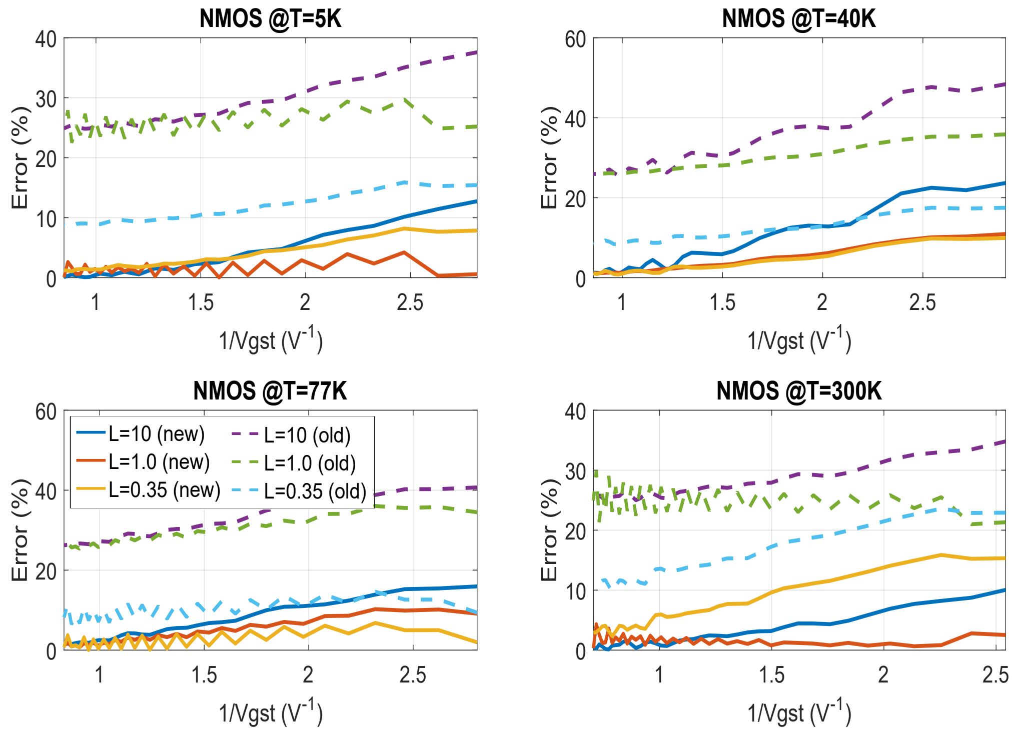


Figure 6.7: Errors between the new model, the conventional model versus measured data of NMOS with W=10μm, L=10, 1, 0.35μm. Error(%) = $100\frac{|model-data|}{data}$.

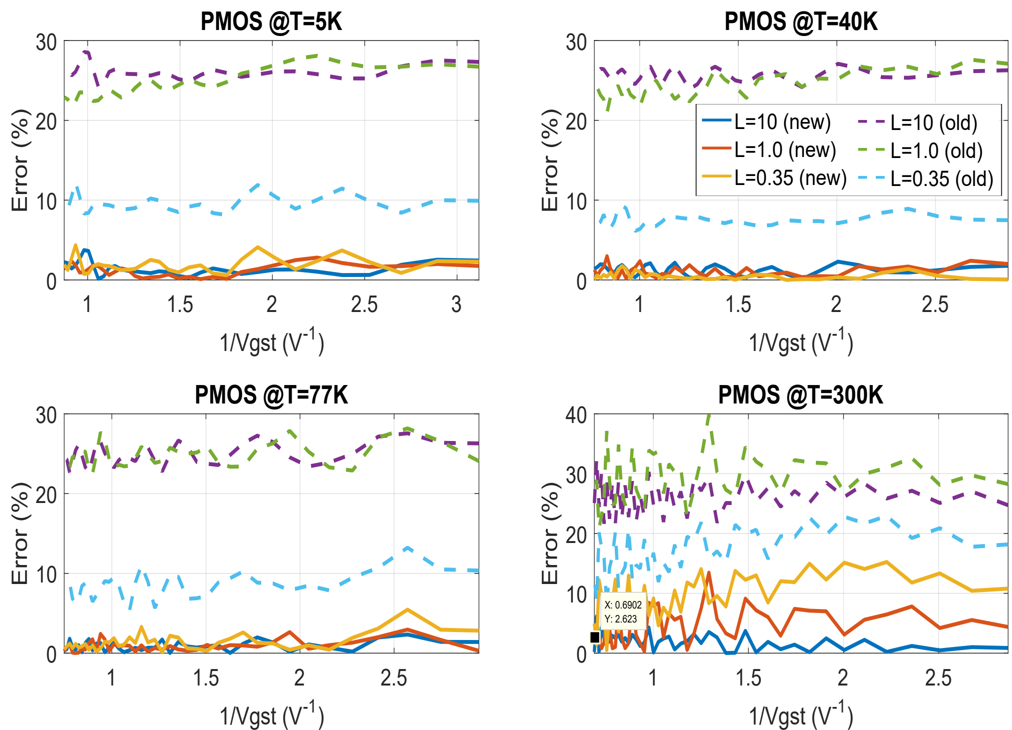


Figure 6.8: Errors between the new model, the conventional model versus measured data of PMOS with W=10μm, L=10, 1, 0.35μm. Error(%) = $100\frac{|model-data|}{data}$.

Table 6.1: Comparison between experimental data vs. the proposed model and conventional model at V_{GST} = 1V
(Error (%) = $100\frac{|\sigma_{\Delta I_D/I_D,Model}-\sigma_{\Delta I_D/I_D,data}|}{\sigma_{\Delta I_D/I_D,data}}$)

T (K)	5	40	77	100	200	300
NMOS W/L = 10/10						
Proposed model (%)	0.19	0.83	1.14	1.16	0.65	0.56
Rahhal's model (%)	11.8	12.42	12.7	12.75	12.29	12.20
NMOS W/L = 10/0.35						
Proposed model (%)	0.72	0.67	0.47	1.08	1.24	2.26
Rahhal's model (%)	4.42	4.36	4.13	4.74	4.89	5.89
PMOS W/L = 10/10						
Proposed model (%)	1.08	0.62	0.16	0.04	1.09	0.05
Rahhal's model (%)	12.51	12.10	11.61	11.69	12.66	11.82
PMOS W/L = 10/0.35						
Proposed model (%)	0.87	0.06	0.20	0.20	1.31	3.55
Rahhal's model (%)	4.59	3.62	3.88	3.88	4.95	7.11

Table 6.2: Variations of parameters and the current at V_{GST} = 1 V

T (K)	5	40	77	100	200	300
NMOS W/L = 10/10						
$\sigma_{\Delta V_{th}}$ (mV)	1.91	1.82	1.76	2.47	2.68	1.58
$\sigma_{\Delta\mu/\mu}$ @V_{GST} (%)	0.89	0.54	0.52	0.75	1.12	0.73
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{GST} (%)	0.39	0.26	0.37	0.67	2.75	3.42
$\sigma_{\Delta I_D/I_D}$ @V_{GST} (%)	0.65	0.4	0.41	0.61	0.97	0.64
NMOS W/L = 10/0.35						
$\sigma_{\Delta V_{th}}$ (mV)	5.07	5.09	5.09	5.01	4.50	4.35
$\sigma_{\Delta\mu/\mu}$ @V_{GST} (%)	0.33	0.26	0.17	0.11	0.06	0.04
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{GST} (%)	1.69	1.45	1.31	1.11	1.78	2.44
$\sigma_{\Delta I_D/I_D}$ @V_{GST} (%)	1.38	1.17	0.99	0.79	0.85	0.70
PMOS W/L = 10/10						
$\sigma_{\Delta V_{th}}$ (mV)	4.78	1.73	1.05	1.18	1.91	2.26
$\sigma_{\Delta\mu/\mu}$ @V_{GST} (%)	6.14	3.08	1.19	0.87	0.51	1.42
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{GST} (%)	1.08	0.85	0.63	0.73	1.37	5.45
$\sigma_{\Delta I_D/I_D}$ @V_{GST} (%)	3.51	2.03	0.90	0.70	0.44	1.25
PMOS W/L = 10/0.35						
$\sigma_{\Delta V_{th}}$ (mV)	4.00	4.42	3.95	4.42	6.75	7.98
$\sigma_{\Delta\mu/\mu}$ @V_{GST} (%)	3.53	1.52	0.39	0.22	0.08	0.06
$\sigma_{\Delta R_{sd}/R_{sd}}$ @V_{GST} (%)	5.31	3.92	2.04	1.79	2.14	2.32
$\sigma_{\Delta I_D/I_D}$ @V_{GST} (%)	4.48	3.48	1.67	1.35	1.10	0.96

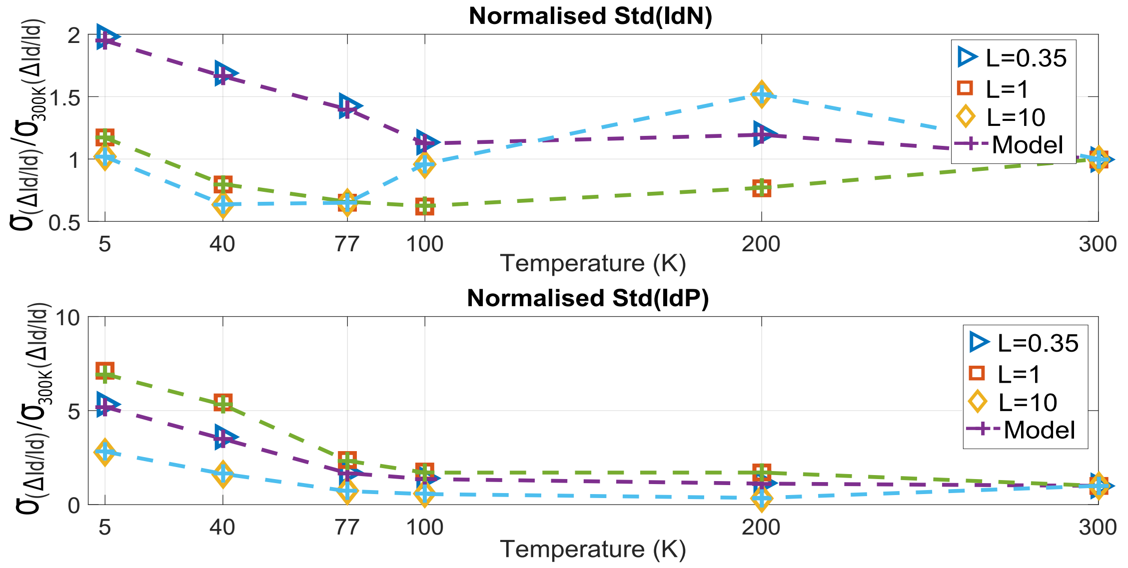


Figure 6.9: Normalised current variations at V_{GST} = 1 V: data (symbol) and model (dash line)

6.4 Geometry effects on transistor matching

As mentioned in Chapter 2, transistors' mismatch due to effects of device geometries is an issue in analog circuit designs. This section reports matching properties of MOS parameters and the drain current as a function of device geometries and temperature.

6.4.1 Effect of device separation distance

In Pelgrom's model (Eq. (2.38)), the device separation distance is one of the dominant factors that influence transistor mismatch. However, thanks to improvements in the fabrication process, this factor has become less significant [123]. In addition, transistors are normally placed close together in practice to minimise the effect of spacing [118]. In order to verify this spatial effect, same-size transistors were placed in a 64x64 array with distances varying from 2 μm to 300 μm.

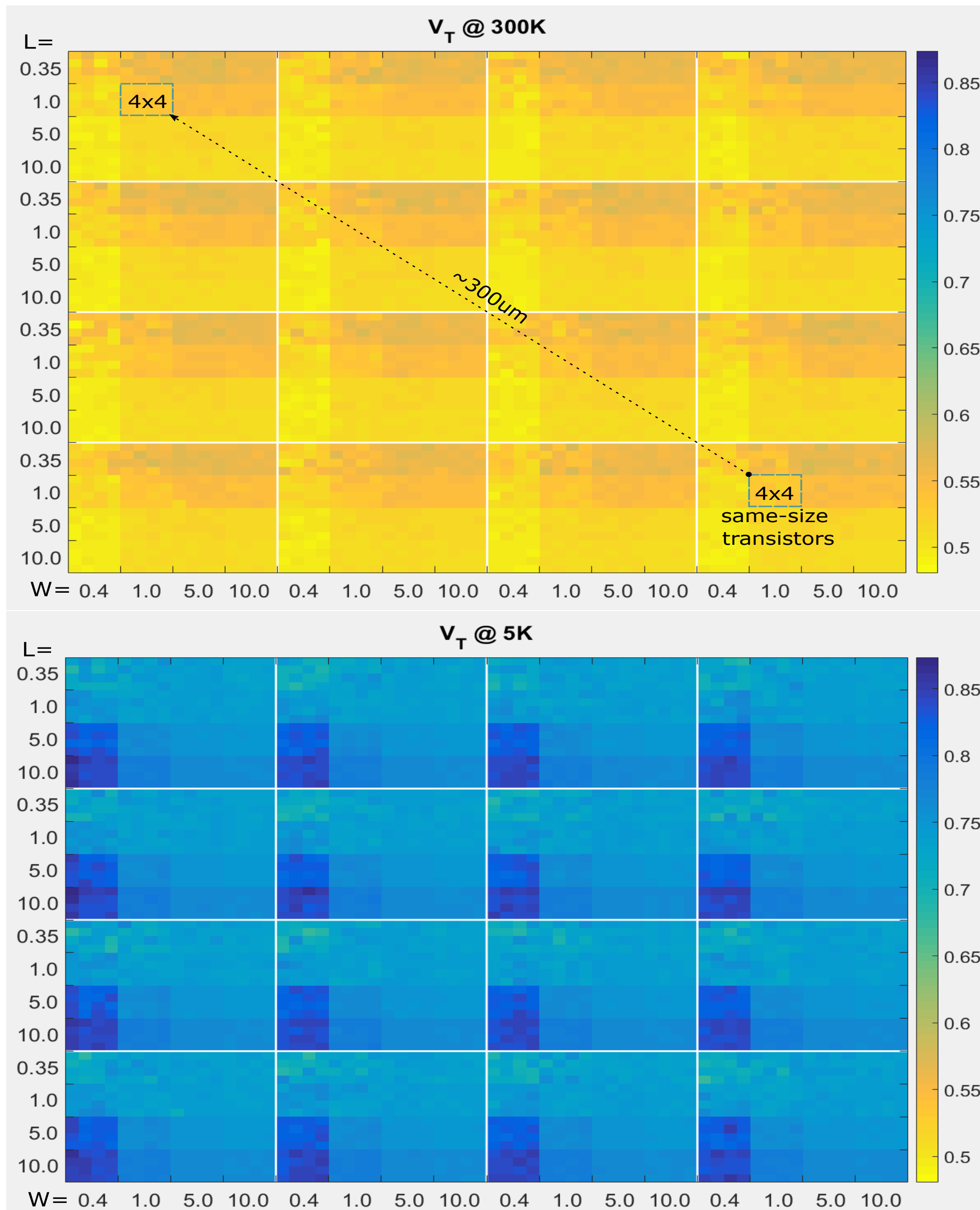


Figure 6.10: Color coded matrix (64x64) of threshold voltage variations at 300 K and 5 K.

Figure 6.10 illustrates distributions of the threshold voltage from the 64x64 transistor array at room temperature and 5 K. No obvious variability correlation among same-size transistor blocks can be observed and V_T variations are less dependent on device distance than the device's size. For example, at 5 K, difference in variation of the threshold voltage of NMOS with W/L =

1/1 [μm] caused by spatial effects is only about 0.9 mV while the difference from device's area (compared to NMOS W/L = 10/10 [μm]) is about 5 mV. Comparisons of V_T fluctuations from different devices at different distances and temperatures are given in Table 6.3. From the results, it can confirm that spacial effect on device mismatch is not significantly affected by temperature and can be ignored. Therefore, A_P becomes the primary factor in regarding device mismatch.

Table 6.3: Variations of threshold voltage at different distances and temperatures

σ_{V_T} (mV)		Temperature	
		300 K	5 K
W/L= 1/1 [μm]	D_x = 300 μm	5.4	6.9
	D_x = 2 μm	4.6	6
W/L= 10/10 [μm]	D_x = 300 μm	1.6	1.2
	D_x = 2 μm	1.7	0.84

6.4.2 Effect of device dimension

According to Pelgrom's model (Eq. (2.38)) and analysis presented in the previous section, variations of MOSFET parameters now can be expressed as a function of the inverse square root of device area. It is written as

$$\sigma(\Delta P) = \frac{A_P}{\sqrt{WL}}, \tag{6.4}$$

where P represents for MOS parameters or the drain current, and A_P is the area proportionality constant.

In order to validate this model, 12 different device dimensions with W/L = 10/10, 10/1, 10/0.35, 5/10, 5/5, 5/1, 5/0.35, 1/5, 1/1, 1/0.35, 0.4/1, and 0.4/0.35 were used in the study.

6.4.2.1 Threshold voltage variation

Pelgrom plots for both NMOS and PMOS transistors are shown in Figure 6.11 and 6.12. Results indicate that the model is still applicable for both device types over a wide range of temperature.

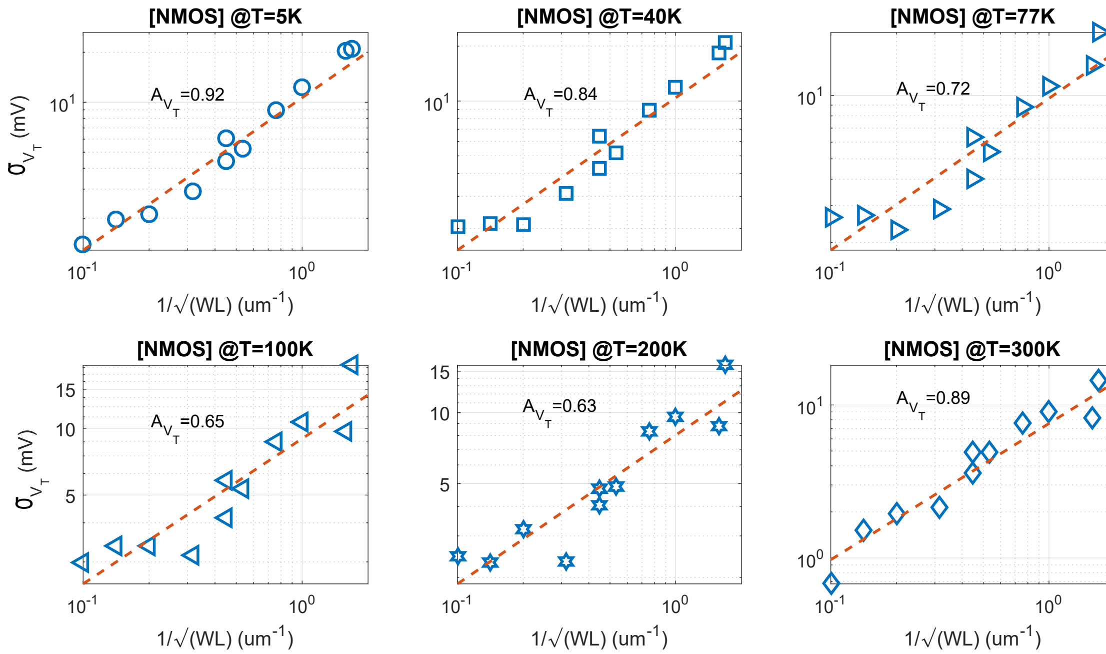


Figure 6.11: Pelgrom plot of σ_{V_T} of NMOS versus the inverse square root of device area.

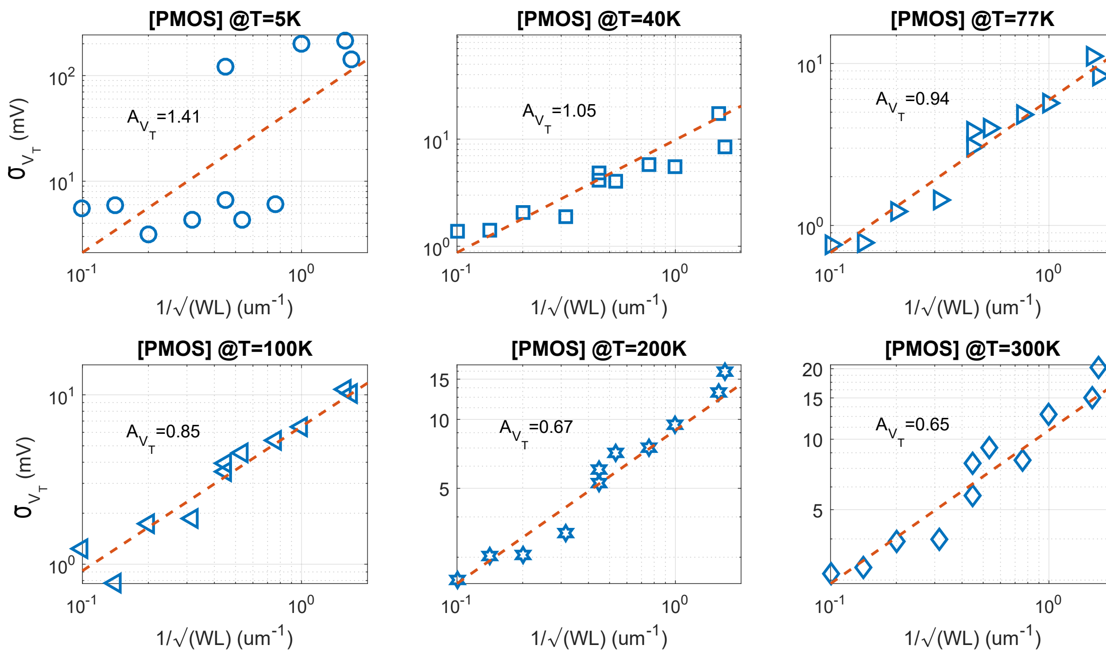


Figure 6.12: Pelgrom plot of σ_{V_T} of PMOS versus the inverse square root of device area.

Only for PMOS transistors operating at 5 K, do the experimental data look inconsistent with

the model. The reason behind this deviation could be because of long-narrow channel effect which might strongly impact variations of the threshold voltage of PMOS at deep cryogenic temperatures.

6.4.2.2 Carrier mobility variation

In the similar way, Figure 6.13 and 6.14 illustrate variabilities of carrier mobility. Results clearly show that the variations are not strictly proportional to $\sqrt{WL}$ at all tested temperatures. This is believed to be because mobility, extracted from the proposed method, is assumed independent of channel length, and impact of series resistance is minimised in the extraction procedure [20]. From the observed results, it can conclude that variations of carrier mobility increase with decreased temperature and reduced device size.

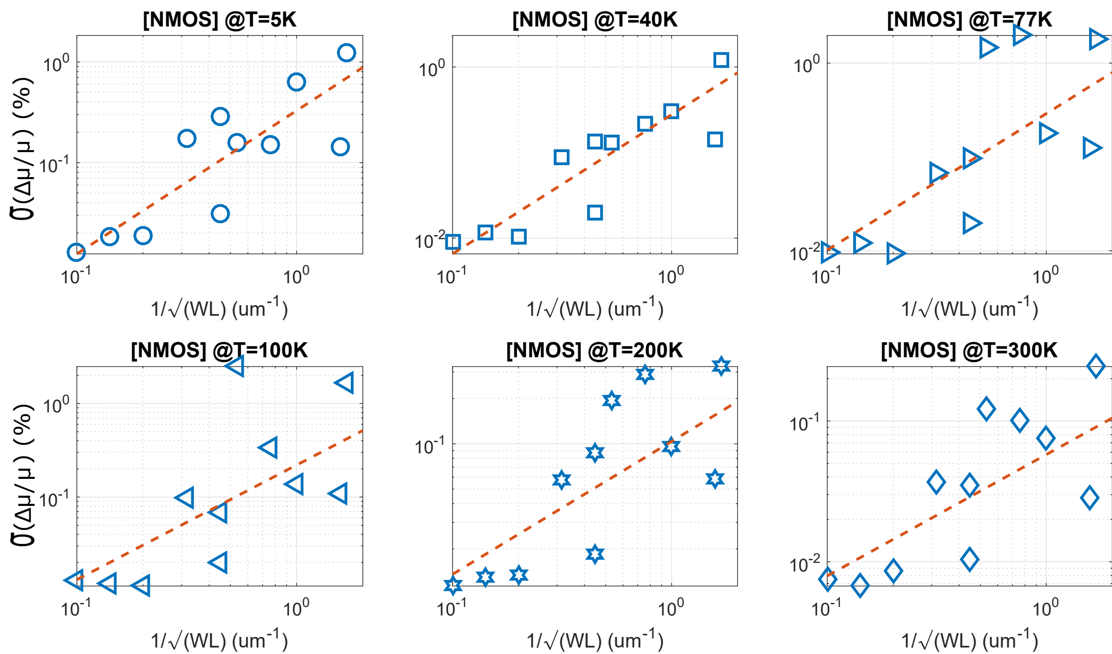


Figure 6.13: Pelgrom plot of $\sigma_{\Delta\mu/\mu}$ of NMOS versus the inverse square root of device area.

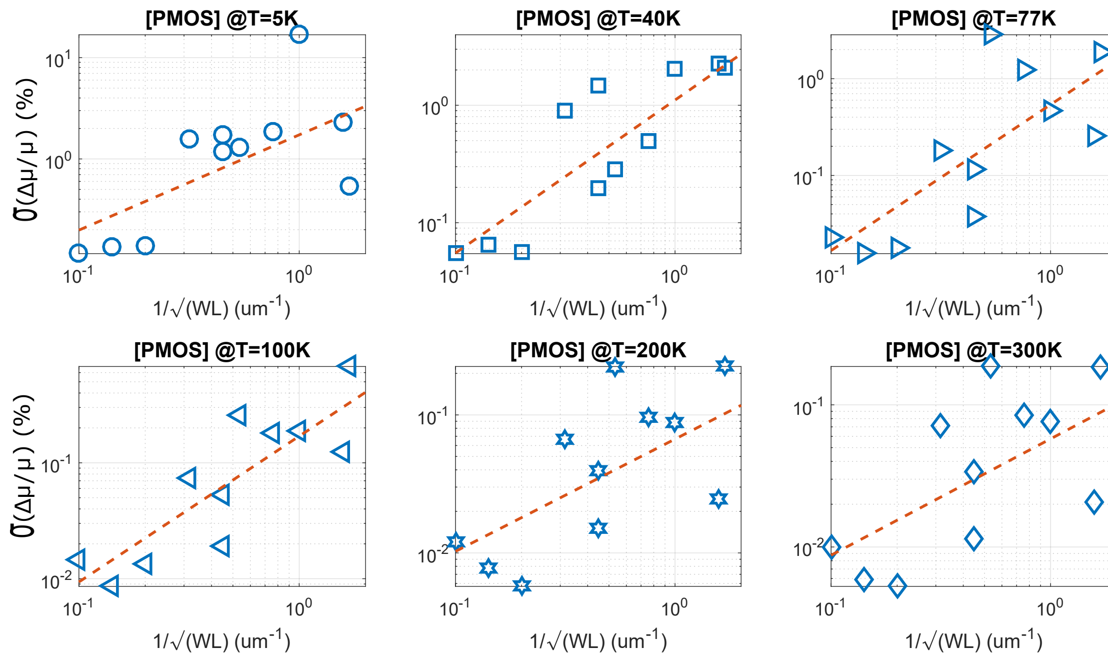


Figure 6.14: Pelgrom plot of $\sigma_{\Delta\mu/\mu}$ of PMOS versus the inverse square root of device area.

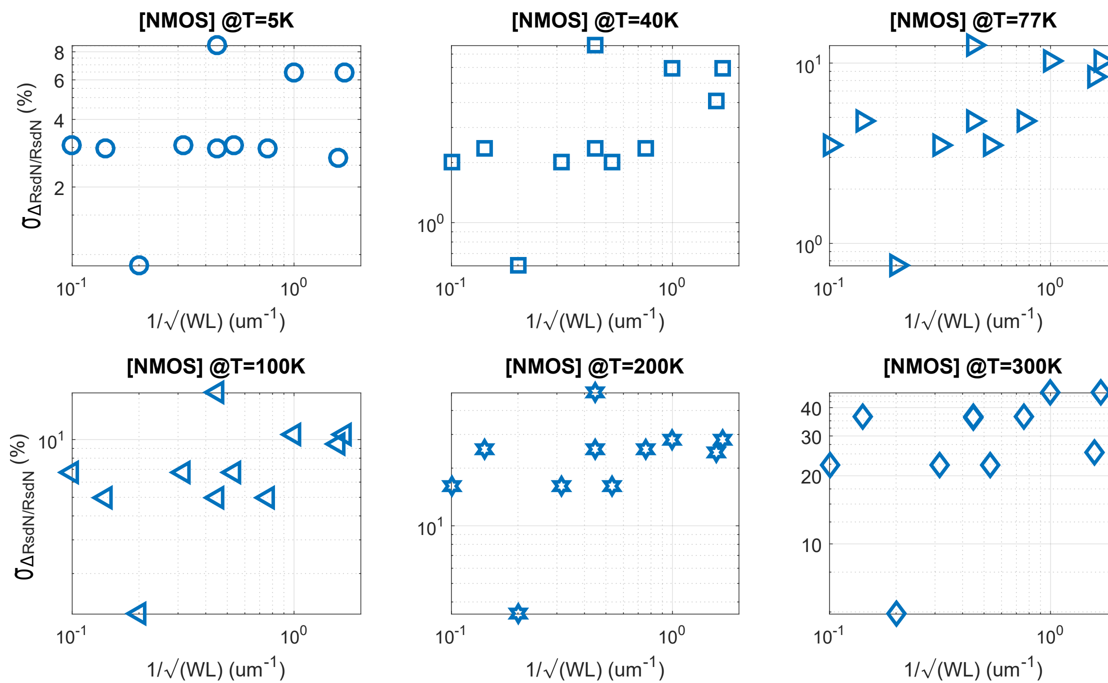


Figure 6.15: Pelgrom plot of $\sigma_{\Delta R_{sd}/R_{sd}}$ of NMOS versus the inverse square root of device area.

6.4.2.3 Series resistance variation

Applying Pelgrom's model, variations of extracted series resistance from NMOS and PMOS are plotted against the inverse square root of device area in Figure 6.15 and 6.16. The observed variations do not follow Pelgom's rule. For both NMOS and PMOS at all examined temperatures, no specific trend of $\sigma_{\Delta R_{sd}/R_{sd}}$ with different device geometries can be revealed. This result agrees with observations in [91].

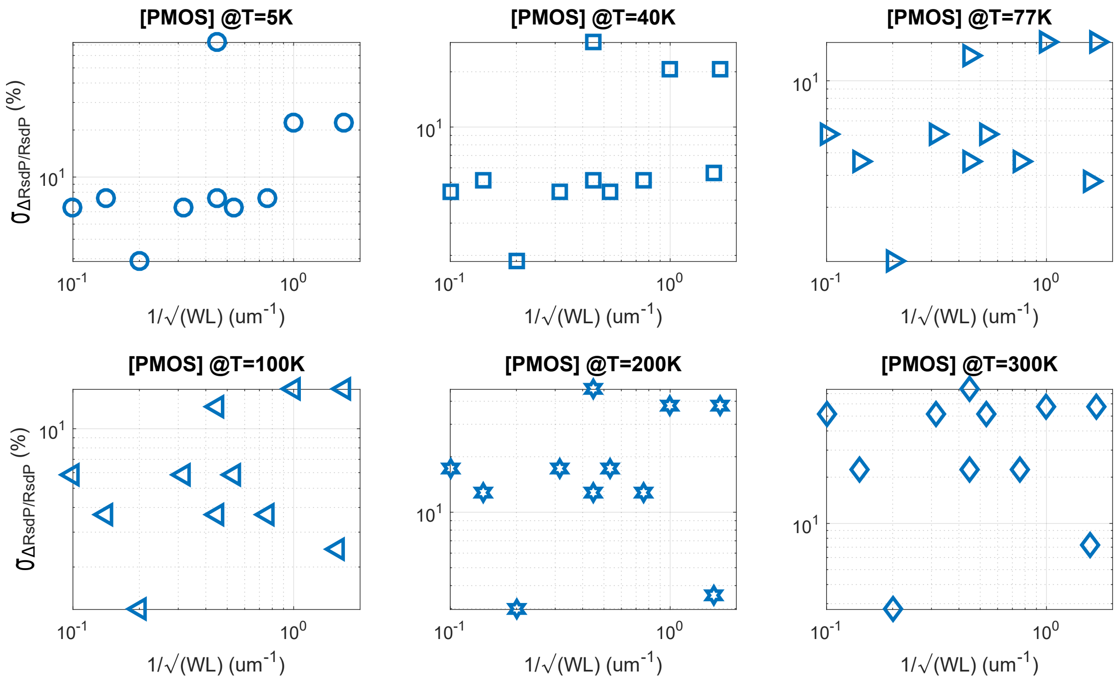


Figure 6.16: Pelgrom plot of $\sigma_{\Delta R_{sd}/R_{sd}}$ of PMOS versus the inverse square root of device area.

6.4.2.4 Drain current variation

Drain current variations of NMOS and PMOS at different temperatures are illustrated in Figure 6.17 and 6.18. The fitting lines on the Pelgrom plots agree with the data from both transistor types. Although fluctuations of the NMOS current at intermediate low temperatures or PMOS current at 5K slightly diverge from the fitting lines, yet, in general, the model is consistent with measurements of drain current with different geometries from 300 K down to 5 K. It can conclude that the drain current mismatch becomes worse with decreased temperature and reduced device dimension.

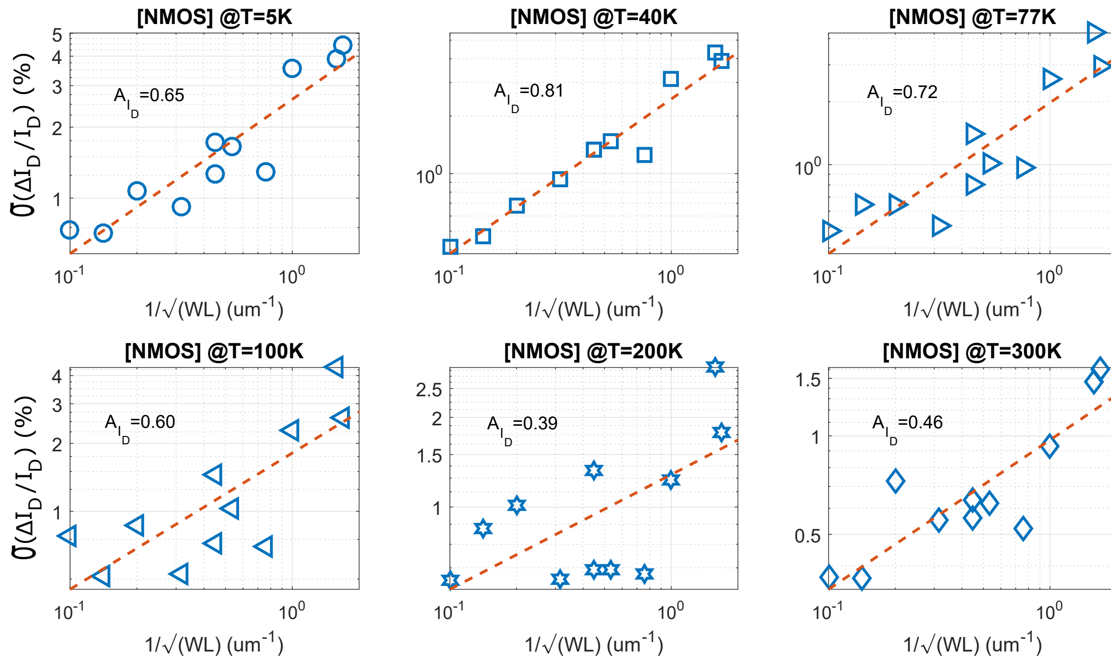


Figure 6.17: Pelgrom plot of $\sigma_{\Delta I_D/I_D}$ of NMOS versus the inverse square root of device area.

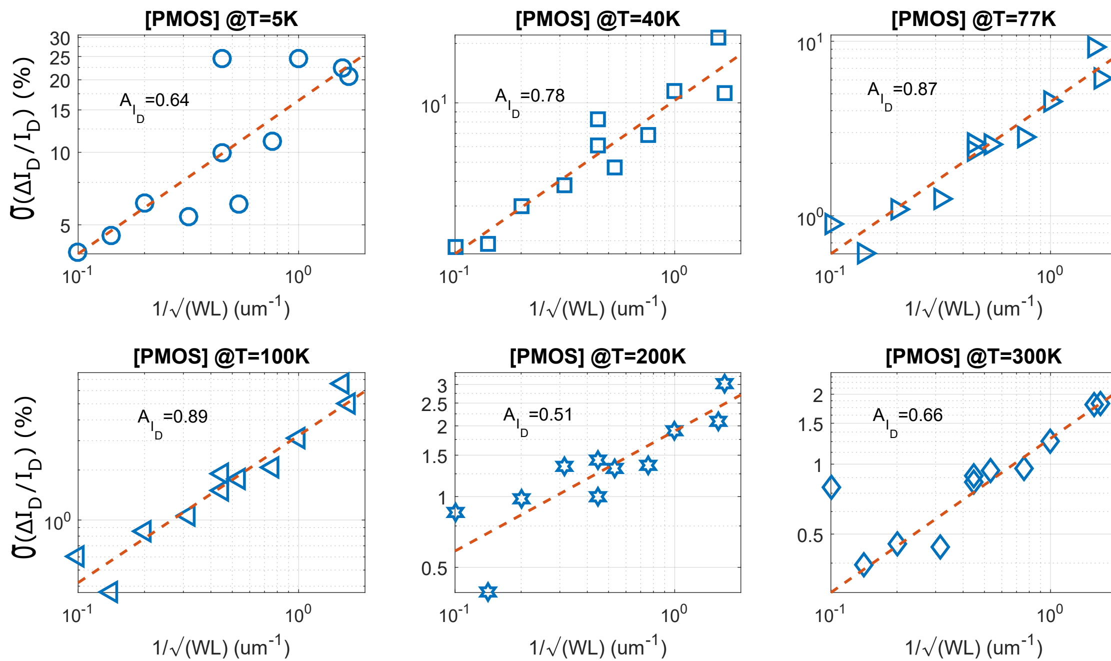


Figure 6.18: Pelgrom plot of $\sigma_{\Delta I_D/I_D}$ of PMOS versus the inverse square root of device area.

6.5 Summary

This chapter has demonstrated the impact of source/drain series resistance on the matching property of the current for the bulk CMOS from room temperature down to 5 K. A new formula to calculate current mismatch, considering series resistance is introduced. The proposed model is simple yet reliable for bulk CMOS characterisation and circuit evaluation over a wide range of temperature. In addition, dependant of MOS parameter variations and drain currents mismatch of bulk CMOS with different device geometries from 5 K to 300 K is presented. Results reveal that matching of transistors becomes worse when device dimension and temperature are reduced.

Chapter 7

Conclusion and Outlook

7.1 Summary of Achievements

Circuits operating at liquid helium temperature for quantum interface and control circuits have recently become important due to renewed interest in quantum computing. Several works have characterised technologies and modelling device at cryogenic temperatures as shown in Chapter 2. Although characteristics of MOS transistors have well reported and explained, a standard model for cryogenic circuit simulation has not existed. The aim of this work has been to characterise and modelling bulk CMOS transistor operations from room temperature down to liquid helium temperature.

As the first step, two test chips, called QNL CMOS and Mulberry, which consisted of transistor arrays were fabricated in the AMS 0.35 μm process (C35, S35). Measurements of devices which were cooled using a cryogenic probe station and dilution refrigerator at temperatures ranging from room temperature down to liquid helium temperature. The experimental setup, test circuits and device measurements were described in Chapter 6.

Parameter extraction is a crucial step in device characterisation. It was a challenge to quantify parameters over a wide range of temperature, especially at deep cryogenic temperatures. In addition, for sub-micron bulk MOSFET transistors, impacts of series resistance due to the source/drain diffusions and the LDD regions, which strongly vary with temperature, must be taken into account. A new approach to extract bulk MOSFET parameters which considers impacts of series resistance was introduced to overcome this problem (Chapter 4).

In order to develop a SPICE model for a wide range of temperature, we examined and modelled temperature dependencies of transistor parameters including a threshold voltage model (Chapter 4), carrier mobility model and model of series resistance (Chapter 5). A SPICE model has been successfully developed based on these temperature dependent parameters (Chapter 5).

The model was coded in the Verilog-A language and required only a single parameter set to predict transistor behaviours at the entire temperature range. This compact model was then tested using the Cadence Spectre simulator.

Another important aspect in studying CMOS characteristics is matching of currents and parameters. Chapter 6 extensively studied matching properties of PMOS and NMOS over the 5 - 300 K temperature range. This work introduced a new formula to estimate the drain current variations and examined MOS parameter variations at cold temperatures. The observed results show that device matching degrades with decreasing temperature and reduced device dimensions.

The contributions of this work are summarised below:

- A new approach to extract source/drain series resistance and MOSFET parameters from 300 K down to 5 K. This approach can separate the effect of series resistance when extracting MOS intrinsic parameters. It was validated in bulk 0.35 μm CMOS and reported in [20].

- A novel threshold voltage model of bulk CMOS operating over a wide range of temperatures. The physic-based model includes effects incomplete ionisation caused by freeze-out carriers at very low temperatures. The model is able to estimate accurately threshold voltage for both long and short channel devices [21].

- A compact model of bulk CMOS for cryogenic circuit simulation. We incorporate threshold voltage model, carrier mobility model and temperature dependence of series resistance into the model. The model is described in the Verilog-A and simulated in a standard simulator. This is the first known model which can replicate bulk CMOS behaviour from room temperature to liquid helium temperature.

- An extensive study of matching properties of MOS transistors was presented. Current variations and parameter variations are examined thoroughly over a wide range of temperature. In addition, a new formula to determine current mismatch for all temperatures was proposed. Our formula and the matching analysis are very useful for circuit evaluation and design for cryogenic applications [20].

7.2 Future Work

Future directions of research can be considered as below:

- Enhance the I-V model for transistor operating in the intermediate inversion and sub-threshold regimes.

- Validate the compact model by evaluating simulation results versus measurements from designed circuits, i.e. ring oscillator, ADC.
- Develop a C-V model for small signal simulation.
- Validate the extraction method using different technologies, i.e. nanometer scale MOSFETs, FDSOI.
- Validate the current matching model and examine parameter variations at low temperatures from different technologies.
- Develop a model for device mismatch and incorporate it into circuit simulator.

7.3 Closing remarks

The aim of this thesis was to characterise and develop a compact model for bulk CMOS device operating over 5 - 300 K. By investigating temperature dependencies of transistor parameters, we were able to develop a wide range temperature transistor model which could be a useful gear for extreme environment circuit designers. This work is also expected to provide a new look on device matching at low temperatures. It can help circuit designers improve the accuracy of their designs, obtain reliable results, and reduce the cost in application development. It is hoped that this work, in a small way, addresses one of the many challenges in achieving useful quantum computing.

Appendix A

I-V Measurements

I-V measurements of PMOS and NMOS at 300 K, 40 K, and 5 K are shown in this appendix. Detailed experimental data for all device sizes and temperatures is available at https://www.researchgate.net/publication/319136011_IdVg_bulkCMOS_AMS_S35_5Kto300K and https://www.researchgate.net/publication/319136315_IdVd_bulkCMOS_AMS_S35_5Kto300K.

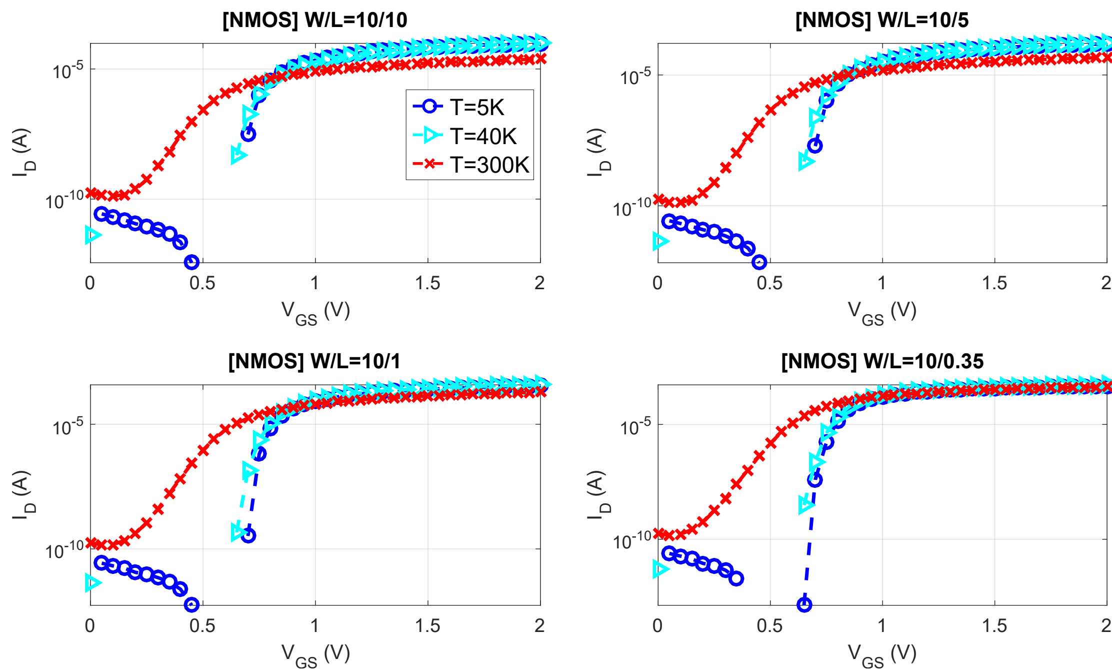


Figure A.1: I_D - V_{GS} of NMOS W=10 μm at V_{DS} = 0.1 V.

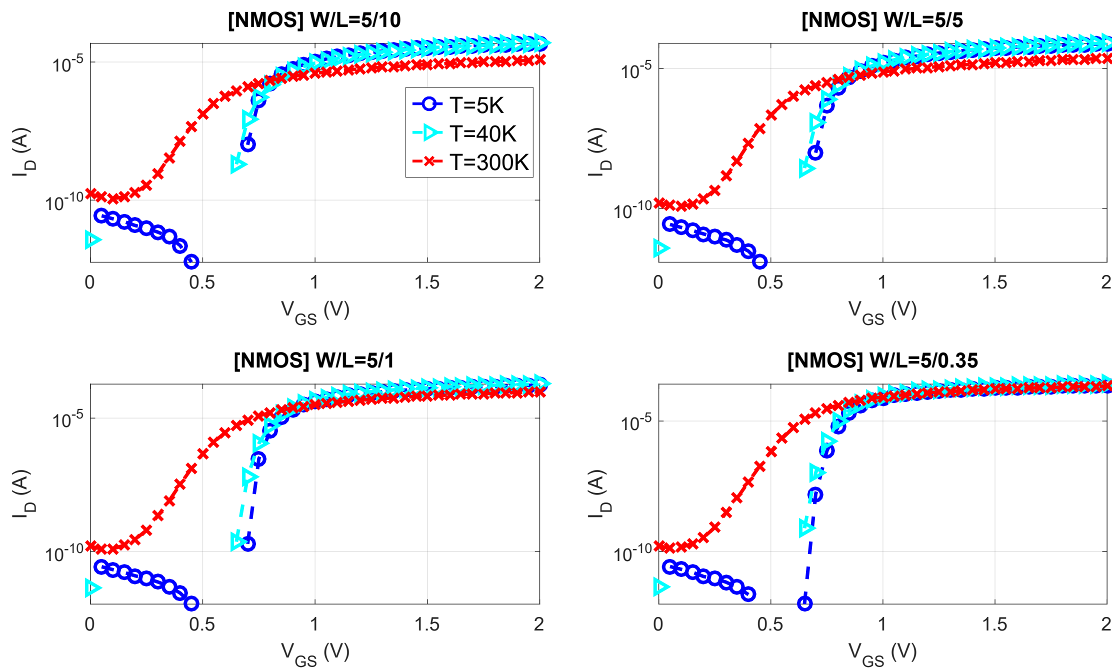


Figure A.2: I_D - V_{GS} of NMOS W=5 μm at V_{DS} = 0.1 V.

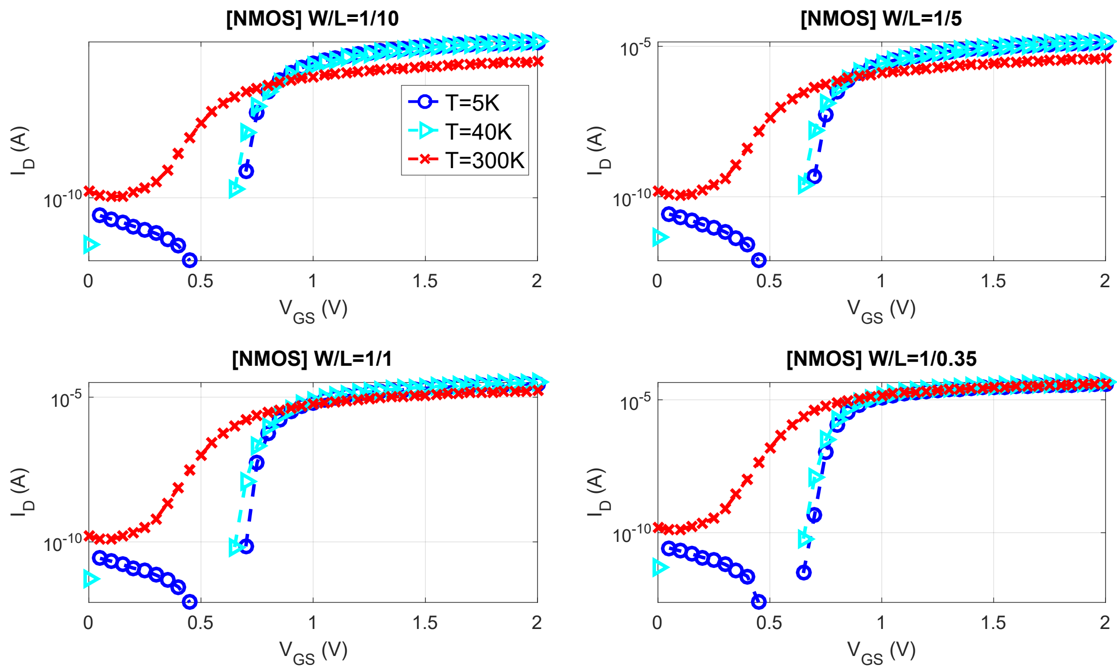


Figure A.3: I_D - V_{GS} of NMOS W=1 μm at V_{DS} = 0.1 V.

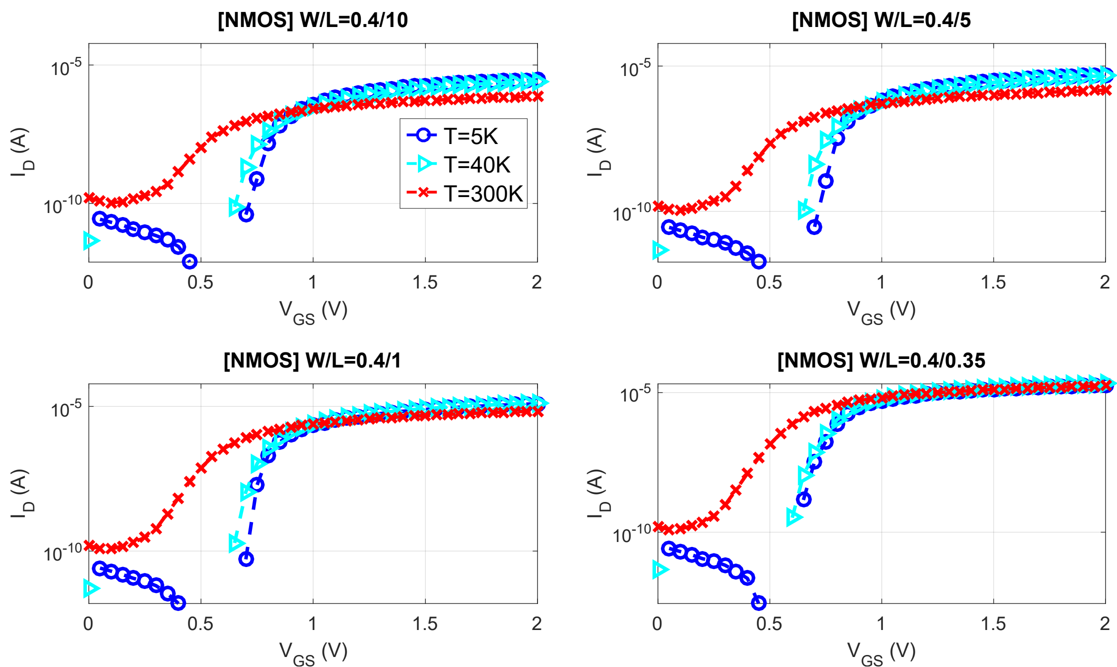


Figure A.4: I_D - V_{GS} of NMOS W=0.4 μm at V_{DS} = 0.1 V.

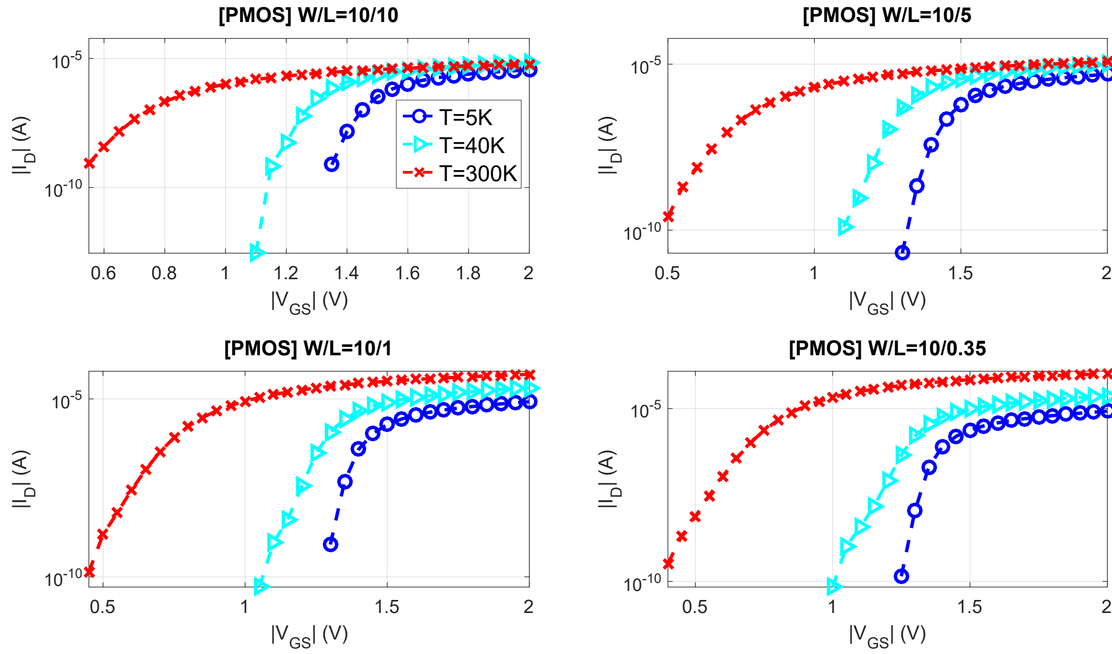


Figure A.5: $|I_D|$ - $|V_{GS}|$ of PMOS W=10 μm at $|V_{DS}|$ = 0.1 V.

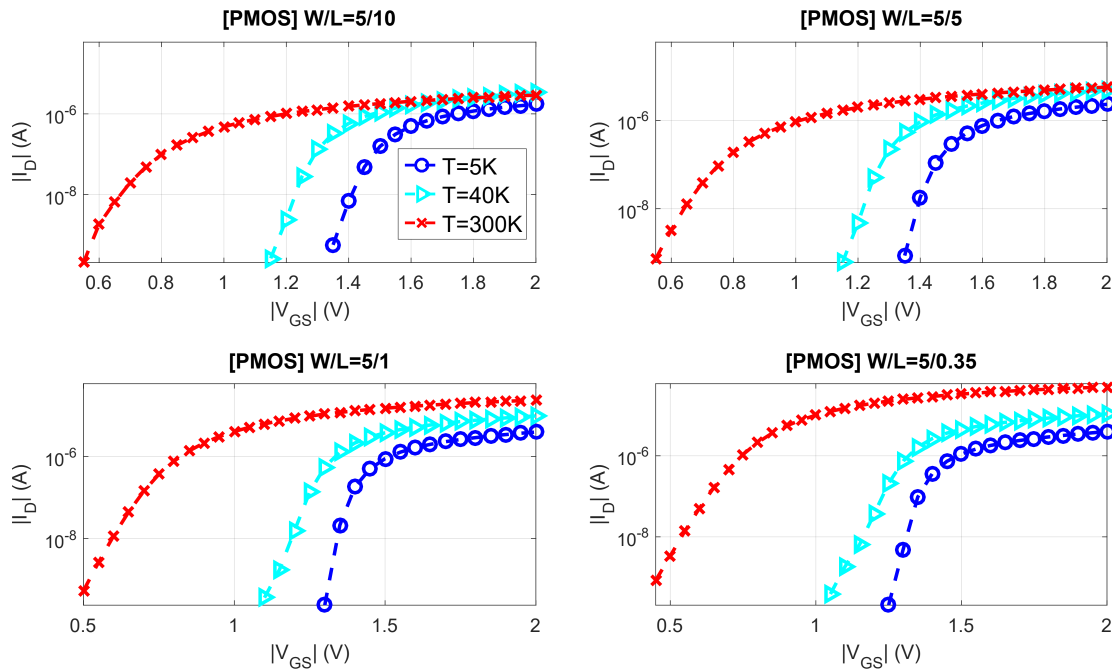


Figure A.6: $|I_D|$ - $|V_{GS}|$ of PMOS W=5 μm at $|V_{DS}|$ = 0.1 V.

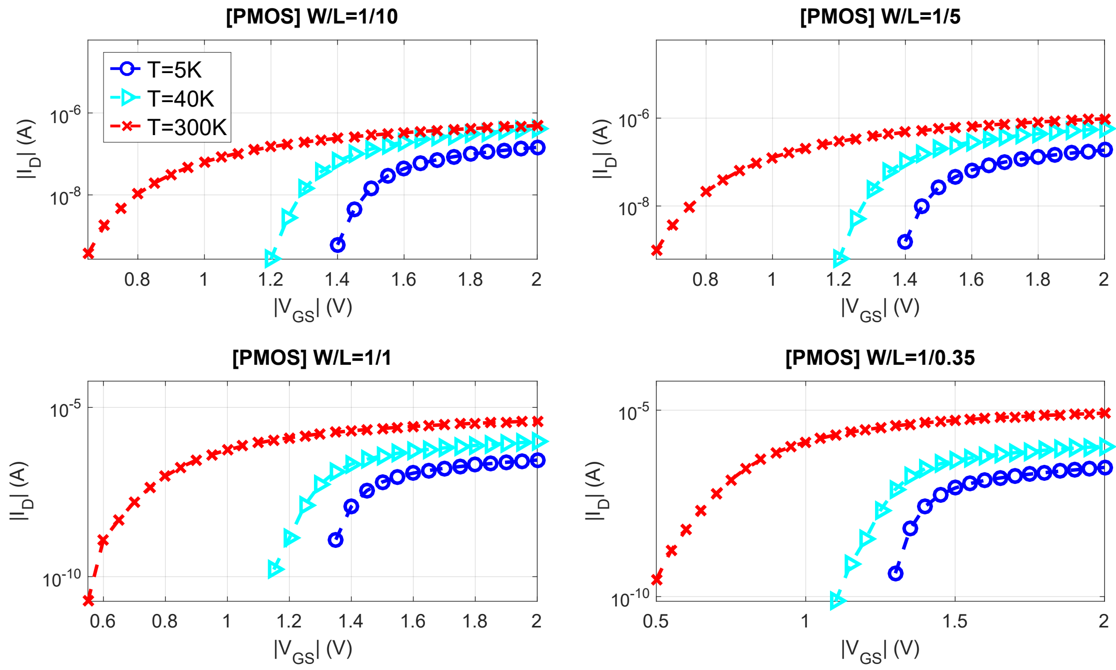


Figure A.7: $|I_D|$ - $|V_{GS}|$ of PMOS W=1 μm at $|V_{DS}|$ = 0.1 V.

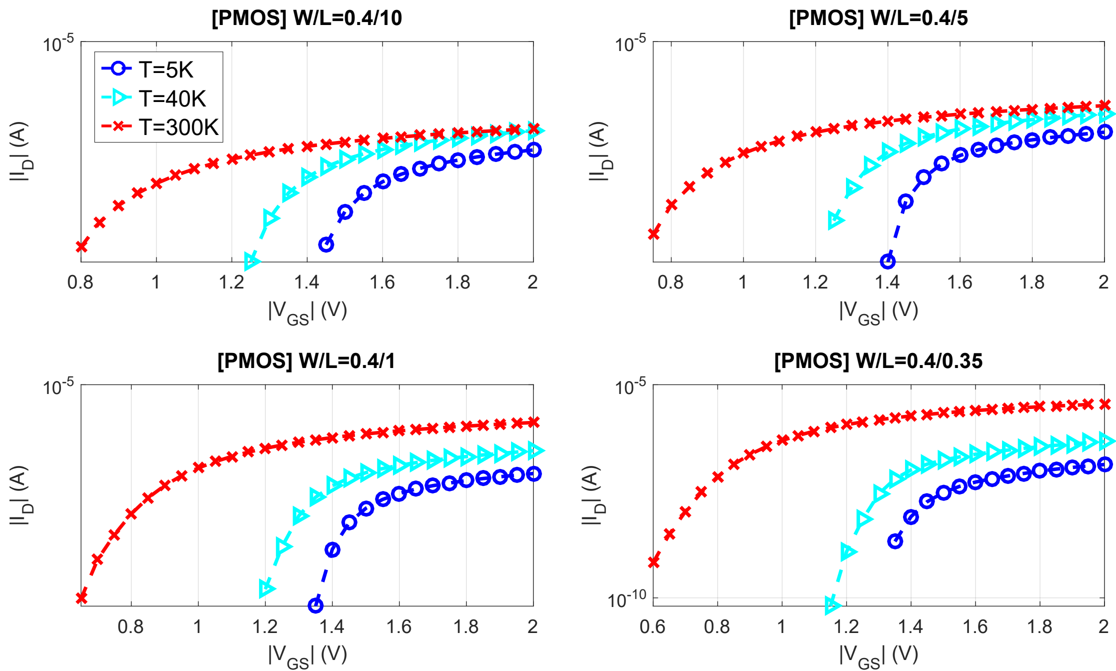


Figure A.8: $|I_D|$ - $|V_{GS}|$ of PMOS W=0.4 μm at $|V_{DS}|$ = 0.1 V.

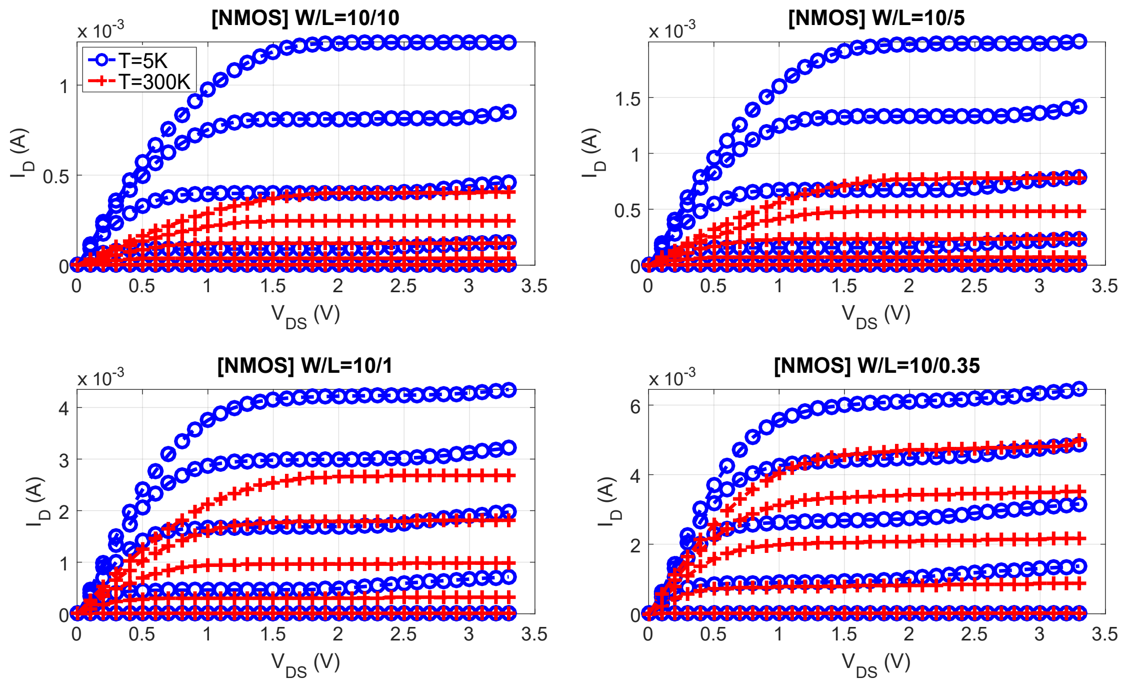


Figure A.9: I_D - V_{DS} of NMOS W=10 μm at V_{GS} = 0.6, 1.2, 1.8, 2.4, 3.0 V.

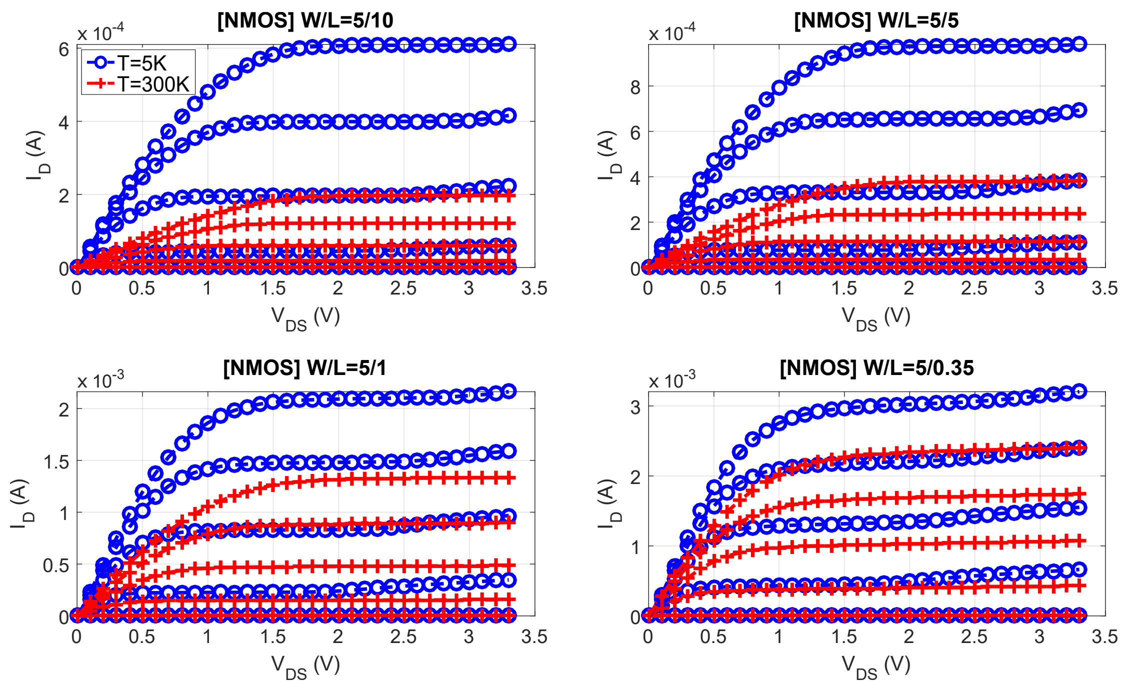


Figure A.10: I_D - V_{DS} of NMOS W=5 μm at V_{GS} = 0.6, 1.2, 1.8, 2.4, 3.0 V.

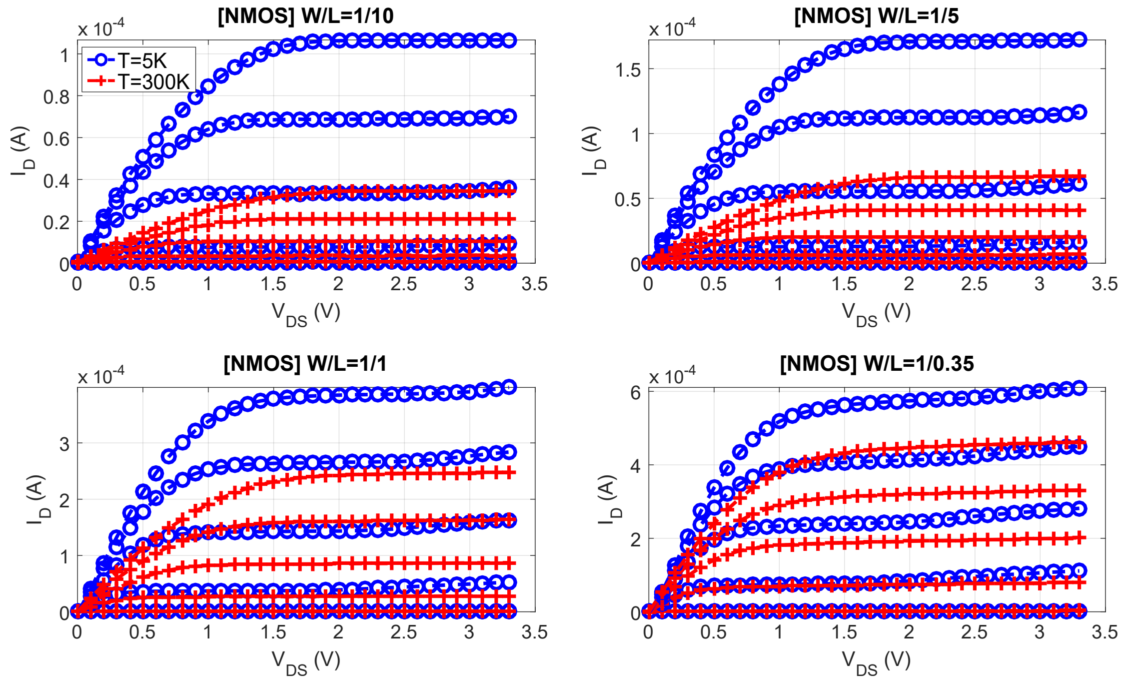


Figure A.11: I_D - V_{DS} of NMOS W=1 μm at V_{GS} = 0.6, 1.2, 1.8, 2.4, 3.0 V.

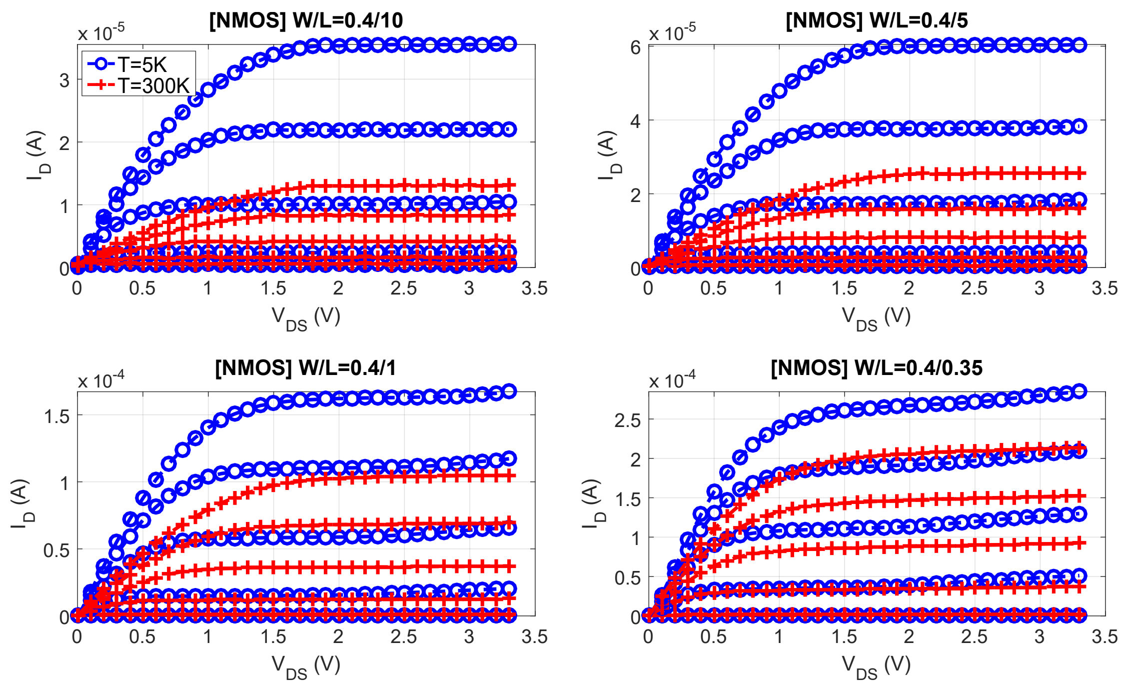


Figure A.12: I_D - V_{DS} of NMOS W=0.4 μm at V_{GS} = 0.6, 1.2, 1.8, 2.4, 3.0 V.

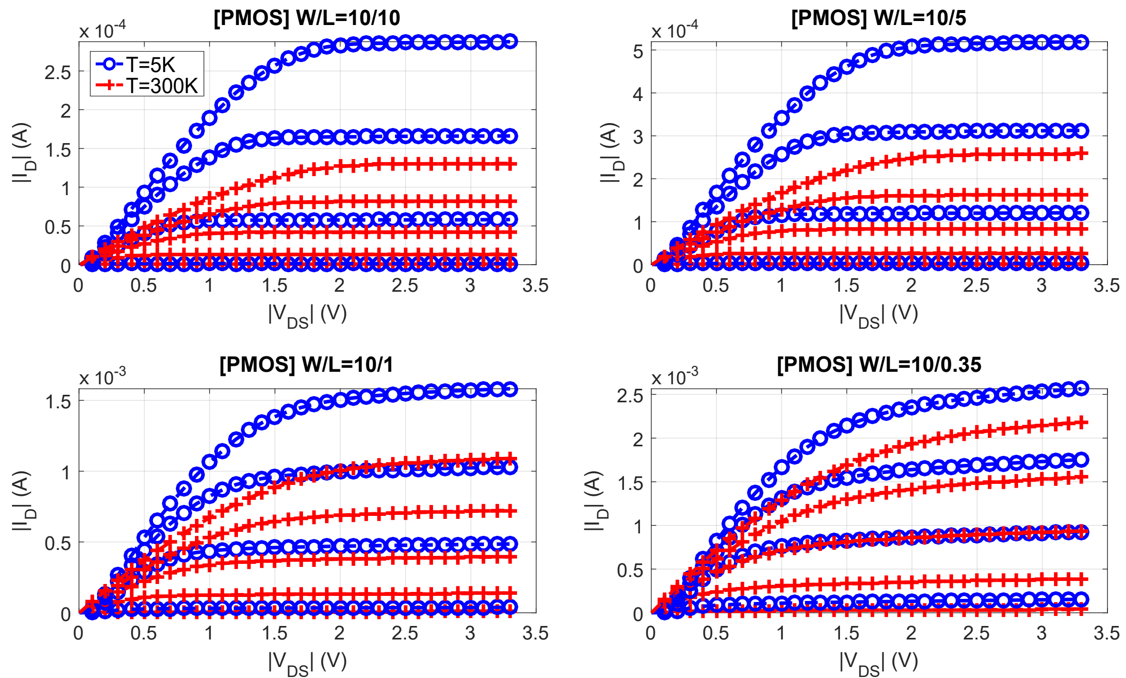


Figure A.13: $|I_D|$ - $|V_{DS}|$ of PMOS W=10 μm at $|V_{GS}|$ = 0.3, 0.9, 1.5, 2.1, 2.7, 3.3 V.

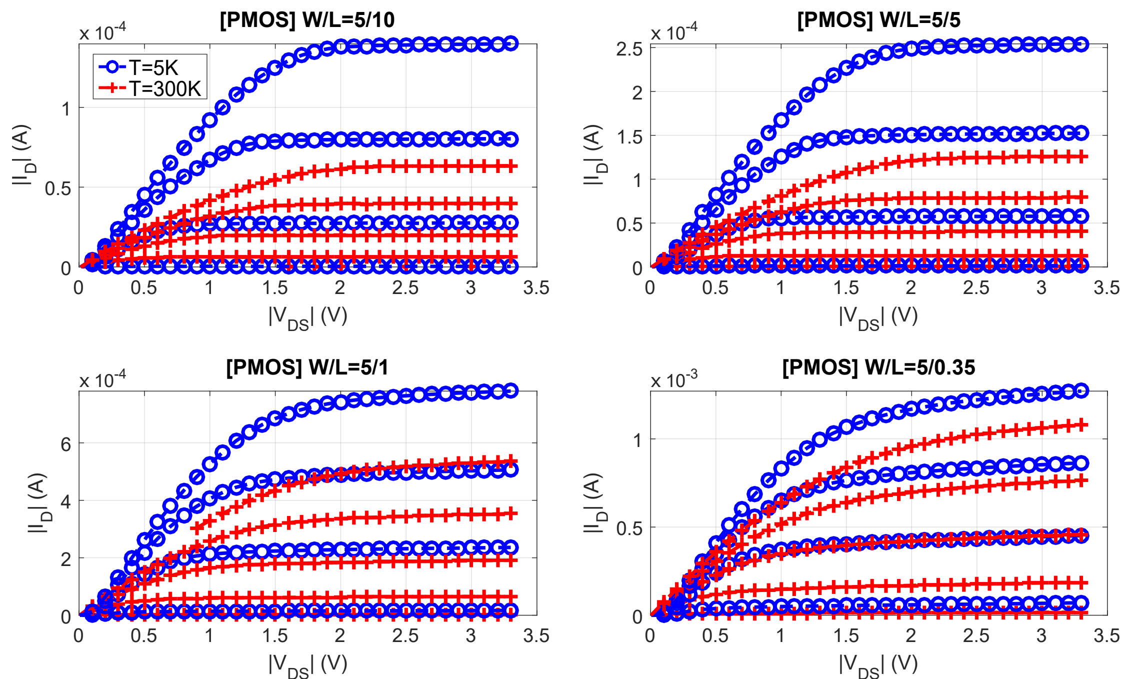


Figure A.14: $|I_D|$ - $|V_{DS}|$ of PMOS W=5 μm at $|V_{GS}|$ = 0.3, 0.9, 1.5, 2.1, 2.7, 3.3 V.

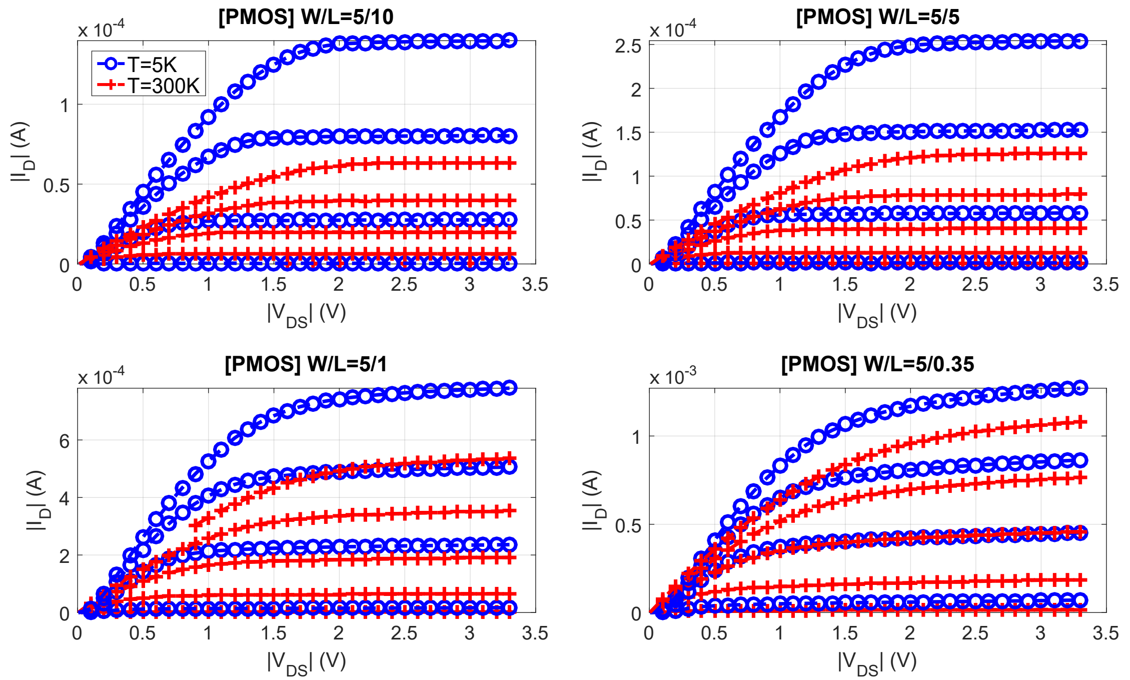


Figure A.15: $|I_D|$ - $|V_{DS}|$ of PMOS W=1 μm at $|V_{GS}|$ = 0.3, 0.9, 1.5, 2.1, 2.7, 3.3 V.

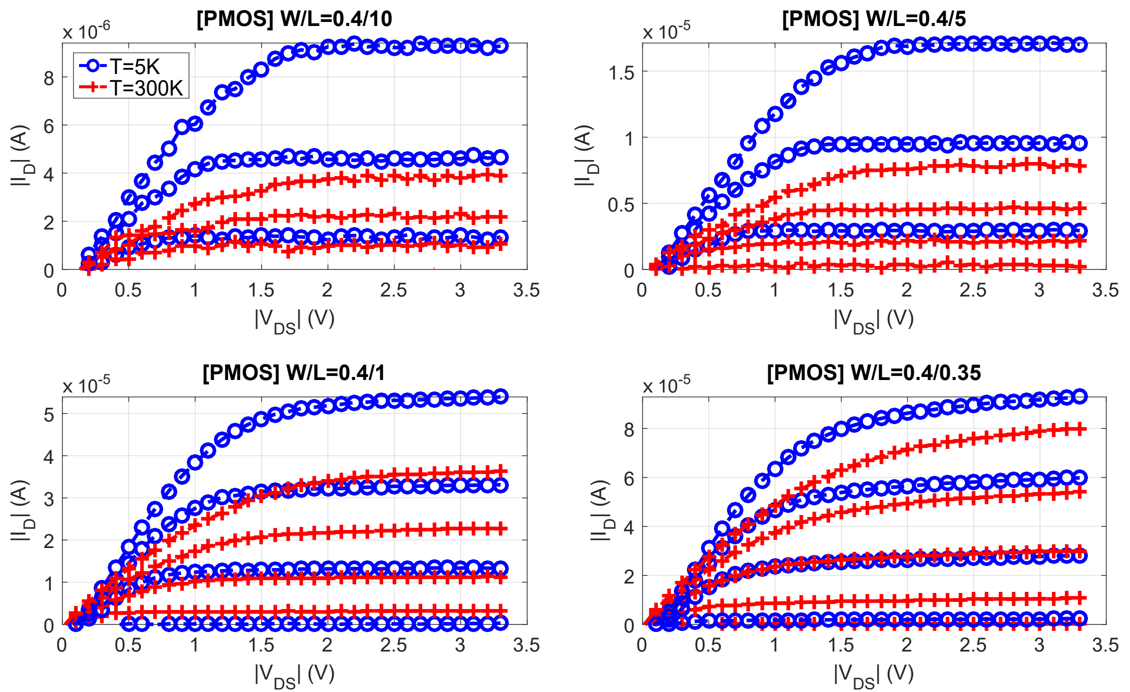


Figure A.16: $|I_D|$ - $|V_{DS}|$ of PMOS W=0.4 μm at $|V_{GS}|$ = 0.3, 0.9, 1.5, 2.1, 2.7, 3.3 V.

Appendix B

Short channel effects and SPICE parameters

B.1 Short channel equations

Equations used in calculation of short channel effects (Chapter 2) at room temperature are referred from BSIM v3.3 [46].

$$\Delta V_T = \Delta V_{Vdop} + \Delta V_{Ldop} + \Delta V_W - \Delta V_{WL} - \Delta V_L - \Delta V_{DIBL} \tag{B.1}$$

Non-uniform vertical doping of the substrate: ΔV_{Vdop}

$$\Delta V_{Vdop} = k_1(\sqrt{\Phi_s - V_{BSeff}} - \sqrt{\Phi_s}) - k_2 V_{BSeff} \tag{B.2}$$

$$k_1 = \gamma_2 - 2k_2\sqrt{\Phi_s - V_{Bm}} \tag{B.3}$$

$$k_2 = \frac{(\gamma_1 - \gamma_2)(\sqrt{\Phi_s - V_{Bx}} - \sqrt{\Phi_s})}{2\sqrt{\Phi_s}(\sqrt{\Phi_s - V_{Bx}} - \sqrt{\Phi_s}) + V_{Bx}} \tag{B.4}$$

$$\gamma_1 = \frac{\sqrt{2q\varepsilon_{Si}N_{ch}}}{C_{ox}} \tag{B.5}$$

$$\gamma_2 = \frac{\sqrt{2q\varepsilon_{Si}N_{sub}}}{C_{ox}} \tag{B.6}$$

where:

V_{Bx} is the substrate bias voltage when the depletion width equals X_t = Φ_s - $\frac{qN_{ch}X_t{}^2}{2\varepsilon_{Si}}$
V_{Beff} = V_{bc} + 0.5[V_{BS} - V_{bc} - δ_1 + $\sqrt{(V_{BS}-V_{bc}-\delta_1)^2-4\delta_1 V_{bc}}$]
δ_1 = 0.001 V
V_{bc} = 0.9(Φ_s - $\frac{k_1{}^2}{4k_2{}^2}$)
Non-uniform lateral doping of the substrate: ΔV_{Ldop}

$$\Delta V_{Ldop} = k_1 \left(\sqrt{1+\frac{Nl_x}{L_{eff}}} \right) \sqrt{\Phi_s} \tag{B.7}$$

where Nl_x = $2L_x(N_{ds}$ - $N_a/N_a)$, N_{ds} is the doping concentration near the drain and the source, and N_a is the doping concentration in the middle of channel.
Narrow effect: ΔV_W

$$\Delta V_W = (k_3 + k_{3b} V_{BSeff}) \frac{T_{ox}}{(W_{eff}+W_0)} \Phi_s \tag{B.8}$$

Short and narrow effect: ΔV_{WL}

$$\Delta V_{WL} = D_{VT0w} \left[e^{-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}} + 2e^{-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}}} \right] \tag{B.9}$$

where L_{wt} = $\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep}}{\varepsilon_{SiO2}}}(1+ D_{VT2}V_{BSeff})$
Short effect: ΔV_L

$$\Delta V_L = D_{VT0} \left[e^{-D_{VT1}\frac{L_{eff}}{2l_t}} + 2e^{-D_{VT1}\frac{L_{eff}}{l_t}} \right] (V_{Bi} - \Phi_S) \tag{B.10}$$

$$l_r = \sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep}}{\varepsilon_{SiO2}}}(1+D_{VT2}V_{BSeff}) \tag{B.11}$$

$$X_{dep} = \sqrt{\frac{2\varepsilon_{Si}(\Phi_s - V_{BSeff})}{qN_{ch}}} \tag{B.12}$$

where V_{bi} is the built-in voltage of the PN junction between the source/drain and the substrate, N_d is the source/drain concentration (or in the LDD regions) if they exist.
$D_V T0$, D_{VT1}, and D_{VT2} are parameters used to make the model fit different technologies.
Drain Induced Barrier Lowering effect: ΔV_{DIBL}

$$\Delta V_{DIBL} = \left[e^{-D_{sub}\frac{L_{eff}}{2l_{t0}}} + 2e^{-D_{sub}\frac{L_{eff}}{2l_{t0}}} \right] (E_{ta0} + E_{tab}V_{BSeff})V_{DS} \tag{B.13}$$

$$l_{t0}\sqrt{\frac{\varepsilon_{Si}T_{ox}X_{dep}}{\varepsilon_{SiO2}}} \tag{B.14}$$

B.2 SPICE parameters

The parameters used in our Verilog-A model are listed as below. We note that these parameters were adapted from MOS BSIM3v3 model (modn - typical mean condition). Meaning of each parameters is given in [46].

Physical constants

EPSOX = 3.453122e-11	KboQ = 8.617087e-5	EPSSI = 1.03594e-10
Qch = 1.60219e-19	NC0 = 5.4078e15	NV0 = 2.0015e15
KB = 8.61733e-5	EAV = 0.044	ECD = 0.046

Process parameters

Tox = 7.575e-9	NA = 2.12e23	ND = 1e26
Cox = 4.5414e-7	dvt0 = 5e1	dvt1 = 1.039
dvt2 = -8.375e-3	dvt0w = 1.089e-1	dvt1w = 6.671e4
dvt2w = -1.352e-2	dsub = 5e-1	eta0 = 1.415e-2
etab = -1.221e-1	k1 = 5.0296e-1	k2=3.3985e-02
k3 = -1.136	nlx = 1.888e-7	w0 = 2.673e-7
Lint = -5e-8	Wint = 9.403e-8	Ll = 0
Lw = 0	Lwl = 0	Lln = 1
Lwn = 1	Wl = 0	Ww = -1.297e-14
Wwl = -9.411e-21	Wln = 1	Wwn = 1
dWg = 0	dWb = 0	

Fitting parameters

TcoeffL = 3.2	ETAa = 1.29	ETAd = 1.45
p0 = 79.68	p1 = 7.51	p2 = 466.6
p3 = -11.46	Um0 = 405	u0 = 1.32
u1 = 0.207	u2 = -1.958	u3 = 2.434
u4 = -1.006	tN10 = -11.7	tN20 = 27.7
Nr00 = 118	Nr01 = -0.0516	Nr02 = -0.0013
Nr03 = -5.326e-7	Nr04 = 1.203e-8	Nr10 = 74.63
Nr11 = -0.5393	Nr12 = 7.296e-4	Nr13 = 1.054e-5
Nr14 = -3.093e-8		

Appendix C

Verilog-A code

```
//=================================================================================//
//  This Verilog-A model is provided "as is", without warranty of any kind and      //
//  you use this model at your own risk.Under no circumstances shall any author     //
//  be liable for direct, indirect, special, incidental, or consequential damages   //
//  resulting from the use, misuse, or inability to use this Verilog-A model.       //
//                                                                                  //
//  Author: Nguyen Cong Dao                                                         //
//  Date: 28/07/2017                                                                //
//=================================================================================//

`include "constants.vams"
`include "disciplines.vams"

module TMOSN(d,g,s,b);

        inout                   d,g,s,b;
        electrical              d,g,s,b;

        branch(d,s)             ds;
        branch(g,s)             gs;
        branch(b,s)             bs;

        //**************************************************//
        // Process parameters
        //**************************************************//
        parameter       real    TNOM    =       300.15;
        parameter       real    DTEMP   =       -0.15;
        parameter       real    Cox     =       4.541e-7;// (F/cm2)
        parameter       real    Tox     =       7.575e-9;
        parameter       real    W       =       10e-6;
        parameter       real    L       =       10e-6;
        parameter       real    NA      =       2.12e17; //substrate doping concentration
        parameter       real    ND      =       1.01e17; //n-well doping concentration
        parameter       real    NC0     =       5.4078e15;
        parameter       real    NV0     =       2.0015e15;
        parameter       real    VQSSN   =       0.4964; //for long transistor Ln=10um
        parameter       real    VQSSP   =       0.0101; //for long transistor Lp=10um
        parameter       real    gamma   =       0.5865; // 0.53*TOX/10*sqrt(NA/1e17)
        parameter       real    gammaP  =       0.4048; // 0.53*TOX/10*sqrt(ND/1e17)
        parameter       real    VTH0    =       0.5156;


        //**************************************************//
        // Fitting parameters
        //**************************************************//
        parameter       real    ETAa    =       1.29;
        parameter       real    ETAd    =       1.45;
        parameter  real   p0            =       79.68;
        parameter  real   p1            =       7.51;
        parameter  real   p2            =       466.6;
        parameter  real   p3            =       -11.46;
        parameter  real   Um0           =       405; //Um at 300K
        parameter  real   u0            =       1.32;
        parameter  real   u1            =       0.207;
        parameter  real   u2            =       -1.958;
        parameter  real   u3            =       2.434;
        parameter  real   u4            =       -1.006;
        parameter  real  tN10           =       -11.7;
        parameter  real  tN20           =       27.7;
        parameter  real  Nr00           =       118;
```

```
parameter  real  Nr01          =       -0.0516;
parameter  real  Nr02          =       -0.0013;
parameter  real  Nr03          =       -5.326e-7;
parameter  real  Nr04          =       1.203e-8;
parameter  real  Nr10          =       74.63;
parameter  real  Nr11          =       -0.5393;
parameter  real  Nr12          =       7.296e-4;
parameter  real  Nr13          =       1.054e-5;
parameter  real  Nr14          =       -3.093e-8;

//*****************************************************//
// Physical constants
//*****************************************************//
parameter      real    KB      =       8.61733e-5;// Boltzmann constant (J/K)
parameter      real    Qch     =       1.602189e-19;// mag. of charge (C)
parameter      real    EPSOX   =       3.453122e-11;
parameter      real    KboQ    =       8.617087e-5;// K/q (eV/K)
parameter      real    EPSSI   =       1.03594e-10;// (F/m)
parameter      real    EAV     =       0.044;
parameter      real    ECD     =       0.046;
parameter      real    EXP     =       2.7183;

//*****************************************************//
// BSIM fitting parameters at 300K
//*****************************************************//
parameter      real    dvt0    =       5e1;
parameter      real    dvt1    =       1.039;
parameter      real    dvt2    =       -8.375e-3;
parameter      real    dvt0w   =       1.089e-1;
parameter      real    dvt1w   =       6.671e4;
parameter      real    dvt2w   =       -1.352e-2;
parameter      real    dsub    =       5e-1;
parameter      real    eta0    =       1.415e-2;
parameter      real    etab    =       -1.221e-1;
parameter      real    k3      =       -1.136;
parameter      real    nlx     =       1.888e-7;
parameter      real    w0      =       2.673e-7;
parameter      real    Lint    =       -5e-8;
parameter      real    Wint    =       9.403e-8;
parameter      real    Ll      =       0;
parameter      real    Lw      =       0;
parameter      real    Lwl     =       0;
parameter      real    Lln     =       1;
parameter      real    Lwn     =       1;
parameter      real    Wl      =       0;
parameter      real    Ww      =       -1.297e-14;
parameter      real    Wwl     =       -9.411e-21;
parameter      real    Wln     =       1;
parameter      real    Wwn =   1;
parameter      real    dWg     =       0;
parameter      real    dWb     =       0;
parameter      real    delta = 0;

real Tdev,Tini;
real NV,NC;
real EV,EC,EG,EA,ED;
real phiF,phiF0,phiFd,phiFTc,phiFdTc,phiS,phiSd;
real fitTemp,Vbi;
real VT,Vth;
real Eeff,MU0,MU;
```

```
real Vbs,Vds,Vgs,Vgst;
real dl,dw1,dw,Leff,Weff,Weff1,Xdep,lt,ltw,lt0;
real k1;
real thetaL,thetaDIBL,thetaWL;
real dVthL,dVthDIBL,dVthWL,dVthW,dVthDop,dVth;
real m,FS;
real phiAFn,phiAFn0,betaN,DeltaG;
real phiAFp,phiAFp0,betaP,DeltaGp;
real Tr,PNt,tN1,tN2,mum,mue,expU;
real Rn0,Rn1,RsdN;
real fn,FB,Vtd,Vds1,Esat;
real Vds0,Vdsat,Vdseff;
real Vgst1,Esat1,Vdsat1;
real vsat,delta_ds,ueff;
real T0l,T0,Idt,Id;

analog begin

        Tini    =       TNOM;
        Tdev    =  $temperature+DTEMP;
        Vbs     = V(bs); //0;
        Vds     = V(ds);
        Vgs     = V(gs);
        $strobe("--- Tdev = %e",Tdev);

        //**************************************************************//
        // Threshold voltage
        //**************************************************************//

        NC      =       NC0*pow(Tdev,1.5);
        NV      =       NV0*pow(Tdev,1.5);
        EG      =       1.16-0.000702*Tdev*Tdev/(Tdev+1108);
        EC      =       EG/2;
        EV      =       -EG/2;
        EA      =       EV + EAV;
        ED      =       EC - ECD;

        phiF = (EA + EV)/2 - ETAa*KboQ*Tdev/2*ln(NA/(4*NV)); //Acceptor (NA)
        //phiFd = (ED + EC)/2 + ETAd*KboQ*Tdev/2.*ln(ND/(2*NC)); //Donor (ND)

        phiFTc = (EA + EV)/2 - ETAa*KboQ*100/2*ln(NA/(4*NV)); //Acceptor (NA), Tc=100K
        //phiFdTc = (ED + EC)/2 + ETAd*KboQ*100/2.*ln(ND/(2*NC)); //Donor (ND)
        phiS    = 2*abs(phiF);
        //phiFSd        = 2*phiFd;

        // Long channel
        VT      =       abs(phiF)-VQSSN+gamma*sqrt(2*abs(phiF));
        $strobe("*** check *** VT = %e, phiF = %e",VT,phiF);
        //VTP   =       abs(PhiFd)-VQSSP+gammaP*sqrt(2*abs(PhiFd));

        //*** Calculate geometrical effects on Threshold voltage (dVth) ***
        // dVth = dVthDop + dVthW - dVthWL - dVthL - dVthDIBL
        // dVthDop: non-uniform lateral doping of the substrate
        // dVthW: narrow effect
        // dVthWL: short & narrow effect
        // dVthL: short effect
        // dVthDIBL: Drain Induced Barrier Lowering effect
        //*************************************************************
        fitTemp = (1-abs(phiF)/abs(phiFTc))*3.2;
        //fitTempP = (1-phiFd/phiFdTc)*3.2;
```

```
Vbi      = 0.0259*ln(1e20/9.65e9) + abs(phiF);
//VbiP   = 0.0259*ln(1e20/9.65e9) + abs(phiFd);

dl = Lint;
dw1 = Wint + Wl/pow(L,Wln) + Ww/pow(W,Wwn) + Wwl/(pow(L,Wln)*pow(W,Wwn));
dw = dw1 + dWg*Vgs + dWb*(sqrt(phiS-Vbs)-sqrt(phiS));

Leff = L - 2*dl;
Weff = W - 2*dw;
Weff1 = W - 2*dw1;

Xdep = sqrt(2*EPSSI*(phiS-Vbs)/(Qch*NA*1e6));

lt = sqrt(EPSSI*Tox*Xdep/EPSOX)*(1+dvt2*Vbs);
ltw = sqrt(EPSSI*Tox*Xdep/EPSOX)*(1+dvt2w*Vbs);
lt0 = sqrt(EPSSI*Tox*Xdep/EPSOX);

thetaL = dvt0*pow(EXP,-dvt1*Leff/(2*lt)) + 2*pow(EXP,-dvt1*Leff/lt);
thetaDIBL = pow(EXP,-dsub*Leff/(2*lt0)) + 2*pow(EXP,-dsub*Leff/lt0);
thetaWL = dvt0w*pow(EXP,-dvt1w*Weff*Leff/(2*ltw)) + 2*pow(EXP,-dvt1w*Weff*Leff/ltw);

dVthL = thetaL*(Vbi - phiS);
dVthDIBL = thetaDIBL*(eta0 + etab*Vbs)*Vds;
dVthWL = thetaWL*(Vbi - phiS);
dVthW = k3*Tox/(Weff1+w0)*phiS;

k1 = sqrt(2*Qch*0.01*EPSSI*NA)/Cox;

dVthDop = k1*(sqrt(1+nlx/Leff)-1)*sqrt(phiS);

dVth = (dVthDop + dVthW - dVthWL - dVthL - dVthDIBL)*fitTemp;

Vth = VT + dVth;
$strobe("*** check *** Vth = %e, dVth = %e",Vth,dVth);
FS = VT/Vth;

//Field-Assisted ionization
m = 1;
phiAFn = (EA-m*phiF);
phiF0 = (EA + EV)/2 - ETAa*KboQ*300/2*ln(NA/(4*NV));//Acceptor (NA), T0=300K
phiAFn0 = (EA-m*phiF0);
betaN = 10.5;
DeltaG = Tox*EPSSI/(4*Qch)*pow(betaN,2)*pow(phiAFn0*Tdev/300-phiAFn,2);

Vth = Vth + DeltaG;
Vgst = Vgs - Vth;


//**************************************************************//
// Mobility
//**************************************************************//
Tr = Tdev/300;
PNt = p0 + p1*Tr + p2*pow(Tr,2) + p3*pow(Tr,3);
tN1 = tN10/PNt;
tN2 = tN20/PNt;
        expU = u0 + u1*Tr + u2*pow(Tr,2) + u3*pow(Tr,3) + u4*pow(Tr,4);
mum = pow(Um0,expU);
mue = mum/(1 + tN1*Vgst + tN2*pow(Vgst,2));
```

```
//***************************************************************//
// Series resistance
//***************************************************************//
Rn0 = Nr00 + Nr01*Tdev + Nr02*pow(Tdev,2) + Nr03*pow(Tdev,3) + Nr04*pow(Tdev,4);
Rn1 = Nr10 + Nr11*Tdev + Nr12*pow(Tdev,2) + Nr13*pow(Tdev,3) + Nr14*pow(Tdev,4);
RsdN = Rn0 + Rn1/Vgst;

//***************************************************************//
// Drain current model
//***************************************************************//

fn = delta*3.14*EPSSI/(2*Cox*10e-6);
FB = gamma*FS/(4*sqrt(abs(phiF0)))+fn;
ueff = mue;

if (Tdev>150) begin
        vsat = 0.70e5;
        delta_ds = 0.18;
end else if (Tdev>70) begin
        vsat =0.85e5;
        delta_ds = 0.150;
end else if (Tdev>30) begin
        vsat =0.95e5;
        delta_ds = 0.160;
end else begin
        vsat =1.18e5;
        delta_ds = 0.10;
end

Esat = vsat/(ueff*1e-4);
T0l = (ueff*1e-4)*Vds/(vsat*Leff);
Vds0 = 0.1;
Idt =  ueff*Cox*W/Leff*(Vgst*Vds0- (1+FB)/2*pow(Vds0,2))/(1+T0l);

Vtd = Idt*RsdN;
Vds1 = Vds-Vtd/2;

Vgst1 = Vgst/(1+FB);
Esat1 = Esat*Leff;
Vdsat = Vgst/(1+FB) + Esat1 - sqrt(pow(Vgst1,2) + pow(Esat1,2));
Vdsat1 = Vdsat-Vds1-delta_ds;
Vdseff = Vdsat - 0.5*(Vdsat1 + sqrt(pow(Vdsat1,2) + 4*delta_ds*Vdsat));

T0 = (ueff*1e-4)*Vdseff/(vsat*Leff*1e6);
Id = ueff*Cox*W/Leff*(Vgst*Vdseff - (1+FB)/2*pow(Vdseff,2))/(1+T0);
//****************
I(ds)   <+      Id;

        end
endmodule
```

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