A Single Chip Carbon Nanotube Sensor

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To my parents, for their love and care.

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Abstract

Recently, carbon nanotubes (CNTs) have been gaining their importance as sensors for chemicals, temperature and fluid flow. Advances in fabrication processes simplify the formation of CNT sensor on silicon substrate, and this provides an opportunity to integrate CNT sensors with CMOS integrated circuits to produce a single chip sensor system.

In this work, two key areas related to single chip CNT sensors were studied, CNT sensor noise and CNT-CMOS integration. CNT sensors were fabricated using DEP force and their noise characterized. Frequency and bias current dependent noise which do not exist in traditional resistive sensors was found. A CNT-CMOS integrated prototype sensor was designed and fabricated using an 0.35 um CMOS process. The prototype included 3 major components, a programmable current source, a dual slope ADC and electrodes for a CNT-based sensor.

The problem of electrode oxidation was identified and a chemical plating process proposed as a solution. It was observed that CNT sensors could be formed on the prototype after plating. An alcohol sensor using our CNT-CMOS prototype was proposed and the feasibility of an integrated single chip alcohol tester demonstrated.

單芯片納米碳管感應器

作者：鄒振德

香港中文大學

二零零七年七月

摘要

近年來，納米碳管被發現在多種感應範疇，例如化學品測試，温度感應及流體速度感應上有鉅大的潛力。技術的進步簡化了納米碳管感應器在硅基底上的制造，這正好提供了很好的機會，讓納米碳管感應器和集成電路整合，成為單芯片感應器系統。

本論文集中研究兩個單芯片納米碳管感應器範疇，分別為納米碳管感應器噪聲及納米碳管感應器之整合。我們量度了納米碳管感應器的噪聲特徵，並發現噪聲受著頻率及偏電流所影響，而這種噪聲並不存在於一般電阻性感應器。我們亦提出了一個將互補金屬氧化物半導體集成電路和納米碳管感應器整合的方法，並制成了一個原形。這原形包括了一個可變電流源、一個雙斜率類比至數位轉換器以及納米碳管感應器電極。

我們發現了鋁納米碳管感應器電極氧化問題及提出了一個化學鍍金解決方案，納米碳管感應器被成功制造在單芯片原形上。最後，我們提出了一個基於單芯片原形的酒精測試機，成功顯示了單芯片納米碳管感應器的可行性。

Acknowledgments

It is impossible to complete this thesis without the help of many people.

I would like to thank Professor Leong Heng Wai Philip, who was my final year and Master Degree supervisor, for his guidance in the past three years, the RA position he provided for the last two years, valuable ideas for my research and opportunities he gave me to learn research methodology.

I would like to thank my Master Degree co-supervisor Professor Li Wen Jung, for the RA position he provided and other financial support to the project. He also provided me many valuable ideas and information about CNT sensors.

I would like to thank Professor Pun Kong Pang, for his comments on the integrated circuit. He also grant me access of the audio analyzer and the Candence® software.

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I would like to thank my colleagues in CMNS, for their help related to CNT sensors, ideas for my research and most importantly, an enjoyable working atmosphere.

Finally, I thank my parents and Mandy, for their love and support.

Statement of Originality

The work described in this thesis was carried out at the Center of Micro and Nano System, the Chinese University of Hong Kong, between 2005 and 2007, under the supervision of Professor Philip Leong and Professor Wen Li.

The work in this thesis is entirely original except where duly referenced. In particular

1. The DEP process for CNT sensor fabrication was developed by Professor Wen Li's research group and the idea of integrating CNT sensor on CMOS process was that of Li and Professor Philip Leong. The sensors used in noise measurement were provided by Ms. Mandy Sin and Ms. Kahlen Ouyang.

2. The CNT formation on the CMOS prototype was joint work with Ms. Pansy Leung and Ms. Carmen Lau.

3. The noise characterization of CNT sensors, the CMOS prototype architecture, design and layout is the work of the author.

4. The idea of chemical plating was that of the author. The entire chemical process was suggested by Chimique Co., Ltd and was executed by the author.

5. All software used for testing was written by the author.

The material in this thesis has not been submitted for any other degree at this or any other institution.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background and Motivation

System-on-a-chip sensors (SOC sensors) are the integration of sensing elements, interfacing circuitry and measurement circuitry in a single integrated circuit (IC). Complementary Metal-Oxide-Semiconductor (CMOS) temperature sensor is an example of SOC sensors [5], where the temperature sensing element and the required circuitry are made within a single CMOS chip.

The major advantages of SOC sensors are reductions in cost and devices' dimensions. Sensors are fabricated using batch fabrication techniques, where hundreds to tens of thousands of them are fabricated on a wafer, hence the fabrication cost is greatly reduced. Devices' dimensions are reduced because they are now fabricated at a micro or nano scale and integrated into a single chip with the electronics. Other advantages of SOC sensors compared with traditional sensor systems include reduction in power consumption and disturbance to the measured environment, increased responsivity and response time [11].

Carbon Nanotubes (CNTs), have been shown to be good sensing elements for pressure, fluid-flow and alcohol [12, 14, 37], and are potential candidates for SOC sensors. However, batch fabrication techniques were not previously available. Recently, a batch fabrication technique using dielectrophoretic (DEP) force was developed by Li. et. al. [13], and this made CNT SOC sensors feasible.

1.2 Objective

The feasibility of CNT SOC sensor has not been demonstrated in past researchs. The main objective of this research is to show that such integration is possible by developing a prototype CMOS IC chip. The detailed aims of the research are:

- Investigate the basic properties of CNT sensors such as noise and self-heating.
- Investigate different CNT sensor measurement techniques.
- Demonstrate the feasibility of CNT-CMOS integration by developing a prototype.
- Discover any difficulties associated with CNT-CMOS integration, and find solution to any potential problems.

1.3 Contributions

The main contributions of this dissertation are:

- The frequency and bias current dependance of CNT sensor noise is characterized. The dominance of low frequency noise was observed and this explained why previous DC measurement techniques used with CNT-based sensors resulted in poor sensitivity [37].
- A CNT-CMOS prototype is developed to show the feasibility of integrating CNT sensors with the associated measurement electronics.
- A major difficulty associated with DEP-based CNT sensor fabrication in standard CMOS process is identified and a partial solution using chemical gold plating was proposed.

1.4 Organization of the Dissertation

Chapter 2 gives an introduction to carbon nanotubes, the fabrication of CNT sensors and other sensor issues. The chapter begins with an introduction to CNTs, and shows the DEP fabrication process for CNT sensor. CNT sensor noise properties and different CNT sensor measurement techniques are introduced.

Chapter 3 gives detail about a CNT-CMOS prototype IC. A review of CNT-CMOS integration is given. The goals are defined followed by the design and analysis of the prototype. Simulation results and the layout of the fabricated IC are also presented. A post fabrication chemical gold plating process required for CNT sensor fabrication is also introduced. Finally, an alcohol tester using the CNT-CMOS integrated sensor is proposed.

Chapter 4 gives results from fabricated CNT-CMOS prototype IC. The testing methodologies of the programmable current source and ADC are presented followed by the testing results. The chemical gold plating process is done on an unpackaged IC, and a CNT sensor is formed on the IC successfully. Testing results of the alcohol tester using carbon film resistors are also presented.

Chapter 5 gives conclusions drawn from the research and directions for the future work.

Chapter 2

Carbon Nanotubes as Sensing Elements

2.1 Introduction

Recently, carbon nanotubes (CNTs) has been gaining their importance for sensing applications [12, 13, 14, 22, 37, 38]. In this chapter, carbon nanotubes are introduced. A dielectrophoretic (DEP) fabrication process is presented which greatly improves the efficiency of CNT sensor fabrication. We also present the thermal noise theory for traditional resistors and show frequency dependent noise measured in our CNT sensor resistance. Frequency dependent noise is not found in traditional resistive sensors and this explains the low accuracy obtained for CNT measurements at low frequencies [37].

We present the working principles of CNT sensors and measurement methodologies which are critical for developing a CNT sensor prototype IC. Finally, we introduce signal to noise ratio (SNR) in CNT measurement, an important figure of merit.

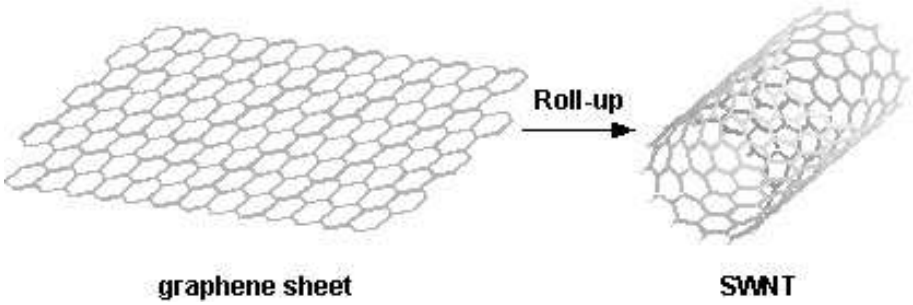

Figure 2.1: An example of SWNT structure [30].

2.2 Introduction to Carbon Nanotubes

Carbon nanotubes (CNTs) were discovered in 1991 by S. Ijiima [18]. They are molecular-scale one dimension tubes of graphitic carbon with some unique properties and can be divided into two categories, namely the **single-walled carbon nanotubes (SWNTs)** and the **multi-walled nanotubes (MWNTs)**. A single-walled carbon nanotube is a sheet of graphite rolled into cylinder with high aspect ratio. Its diameter in the order of nanometers and its length may vary from tens of nanometers to few millimeters (Fig 2.1). A multi-walled CNT is similar to single-walled CNTs but has more than one rolled sheet in the cylinder. Due to their unique molecular structure, CNTs are one of the stiffest and strongest materials [43], they are one of the most effective thermal conductors [2] and also have many novel electrical and optical properties. These unique characteristics makes CNTs potentially useful in a wide variety of applications in nanotechnology, sensors, actuators, electronics and optics.

A CNT can be either metallic or semiconducting, the chirality being the key to this electric property, Fig 2.2 illustrates chirality which is represented by a pair of indices (n, m) called the chiral vector [30]. The integers n and m denote the number of unit vectors along two the directions in the honeycomb crystal lattice of graphene. If $m = 0$, the nanotubes are "zigzag" and if $n = m$, the nanotubes are "armchair". Otherwise, they are called "chiral". In a SWNT, if $(n - m)$ is multiple of 3, then it is metallic, otherwise it is semiconducting.

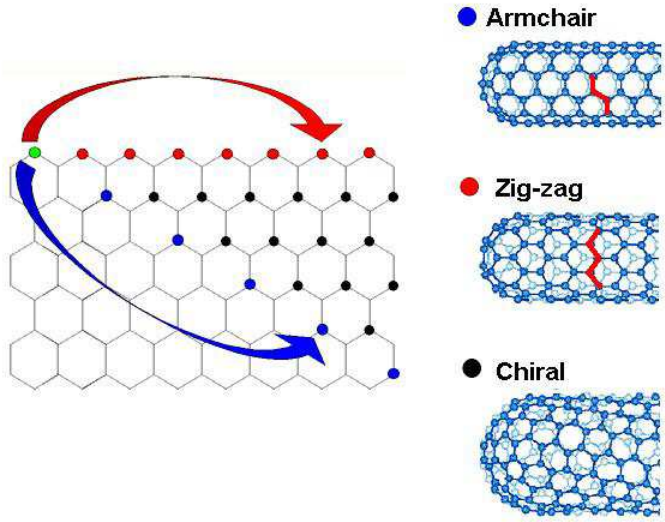

Figure 2.2: Chirality in carbon nanotubes. Imagine the hexagonal lattice being rolled such that the green dot (carbon atom) matches up with another colored atom. Each color (red, blue, black) corresponds to a different structure [41].

2.3 Fabrication of Single Carbon Nanotube Sensors

CNTs tend to cling together in nature due to the presence of strong surface charges. Thus, we have to go through some fabrication procedures to fabricate **single CNT** sensing elements. This includes isolation of single CNT, aligning the CNT to the desired location, fixing the CNT and making electric connections. As the dimension of CNTs are molecular in order, AFM (Atomic force microscope)-based assembly is commonly used for fabrication [36, 42]. However, the cost and inefficiency of AFM-based assembly prevents single CNT sensors from being used in practical sensing applications.

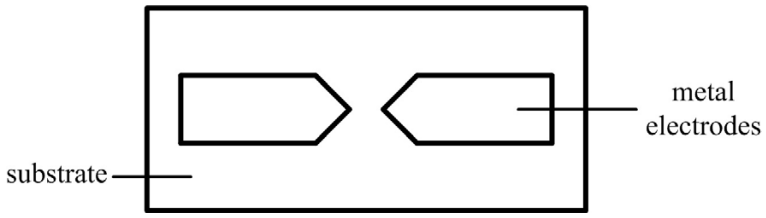

Figure 2.3: Electrodes for CNTs sensor formation.

2.4 Batch Fabrication of CNT Sensors using Dielectrophoretic Force

To remedy the fundamental difficulties of manipulating single CNTs, some researchers treat bundles of CNTs as sensing elements. By combining the chemical vapor deposition (CVD) with lithography [47] or laser trimming [6] techniques, "vertically" aligned CNTs can be grown and patterned on a specific site in a batch process.

Electric field assisted batch fabrication is another promising method to manipulate CNTs bundles. Yamamoto, et al. demonstrated the possibility to manipulate CNT using AC electric field [49]. Wen Li and his research group, invented the methodology to fabricate bundle CNTs sensing element using dielectrophoretic (DEP) force [13]. This methodology is simple and effective, can produce CNTs bundles of sensing elements and is compatible with commercial CMOS process. We will describe the principle of DEP fabrication in the following sections.

2.4.1 Basic CNTs Sensor Fabrication Process using DEP Process

Dielectrophoresis is a phenomenon where neutral particles undergo mechanical motion inside a nonuniform ac electric field [34]. To fabricate CNT sensors using Li's process [13], we prepare a pair of metal electrodes (usually gold) on a substrate (Fig. 2.3). The separation between the electrodes should be small enough

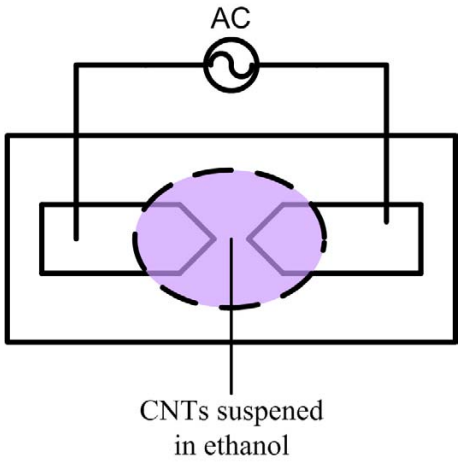

Figure 2.4: Apply AC voltage between CNT electrodes.

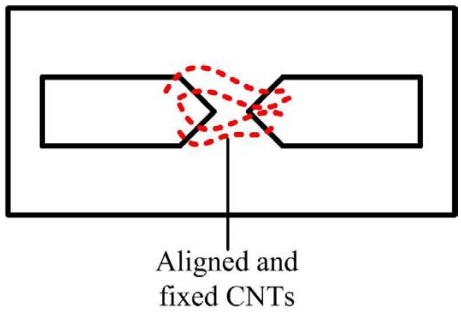

Figure 2.5: CNTs bundles aligned and fixed between electrodes, a CNT sensor formed

so that significant DEP force is generated. Experimental result show that this separation should be at most $\sim 100um$. Secondly, bundles of CNTs (in powder form) should be ultrasonically dispersed in buffer solution (e.g. ethanol), a droplet of this solution is put between the gap of the electrodes, and finally, an AC voltage is applied to the electrodes to generate the DEP force (Fig. 2.4). After few minutes, the ethanol is evaporated and a CNT sensor is formed between the electrodes (Fig. 2.5).

The advantages of this CNT sensor fabrication process are:

- CNTs are not grown on the substrate, they are just aligned and fixed during the process. Thus commercial CNTs can be used and the expensive CNT growth process is avoided.

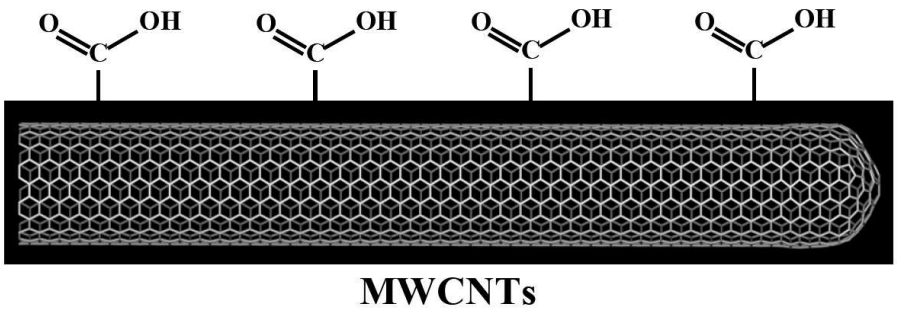

Figure 2.6: A MWNT functionalized by COOH group.

- The precision requirements of the electrodes (few um to a hundred um) is easily achieved with modern photolithography techniques or any modern CMOS process.
- The process can be automated and produced in batches using existing automated micro-spotting techniques [23].

2.4.2 Modification of Fabrication Process

As carbon nanotubes are made from carbon atoms, we can introduce other functional molecules in order to alter their properties. This process is called functionalization. By attaching COOH functional group molecules to a CNT, the sensitivity of CNT to alcohol will increase [38]. An illustration of a functionalized MWNT is shown in Fig. 2.6. We can use functionalized CNTs to fabricate CNT sensors with different properties to pure CNTs.

2.5 Noise in Resistors

Noise is an important factor which limits the sensitivity of a sensor. Before we study noise in CNT sensors fabricated by DEP process, it is important for us to understand noise in traditional resistors.

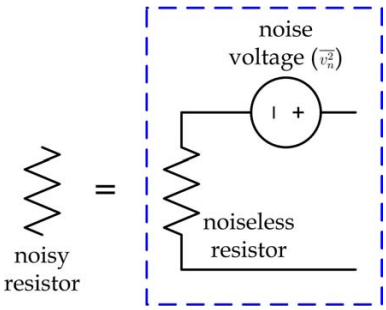

Figure 2.7: Voltage noise model of resistor.

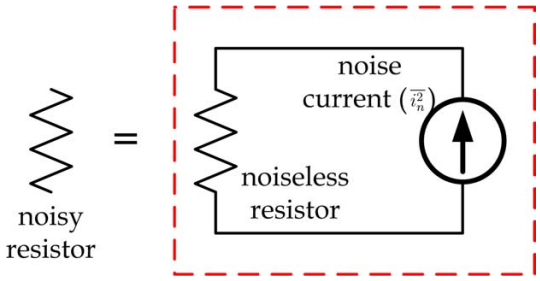

Figure 2.8: Current noise model of resistor.

2.5.1 Thermal Noise in Traditional Resistors

It is well known that thermal noise dominates in a resistor [15]. A resistor with thermal noise can be modeled by a noiseless resistor with a noise voltage source (Fig. 2.7) or a noiseless resistor with a noise current source (Fig. 2.8). The mean squared noise voltage and current is modeled by Eq. 2.1 [15]:

$$\begin{aligned} \overline{v_n^2} &= 4kTR\Delta f \\ \overline{i_n^2} &= 4kT\frac{1}{R}\Delta f \end{aligned} \tag{2.1}$$

where

$\overline{v_n^2}$ is the mean squared voltage noise

$\overline{i_n^2}$ is the mean squared current noise

k is Boltzmann's constant

T is absolute temperature (in Kelvin)

R is resistance of the resistor

Δf is the noise bandwidth (in Hz)

From the equations, we note that thermal noise depends on the resistance of the resistor (R) and is directly proportional to the absolute temperature (K). The spectral density of thermal noise is independent of frequency, and produces white noise where the spectral density is the same at any frequency.

2.5.2 Flicker Noise ($1/f$) Noise in Traditional Resistors

Flicker noise ($1/f$ noise) exists in all active devices such as diodes, bipolar transistors, CMOS transistors and some passive devices such as carbon resistors [10], it can be represented by the following equation [15]:

$$\overline{i_n^2} = K_1 \frac{I^a}{f^b} \Delta f \tag{2.2}$$

where

Δf = small signal bandwidth (in Hz)

I = conducting current

K_1 = constants depending on device

a = current dependance (a constant in the range 0.5 to 2)

b = frequency dependance (a constant of about unity)

The equation shows that spectral density of flicker noise is inversely proportional to frequency. Fig. 2.9 shows the frequency dependance of thermal noise and flicker noise.

2.6 Noise in CNTs Resistors

2.6.1 Literature Review

Carbon atoms are the major components of CNTs, hence the flicker noise of carbon resistors may also exist in CNT sensors. Collins, et al. reported bias

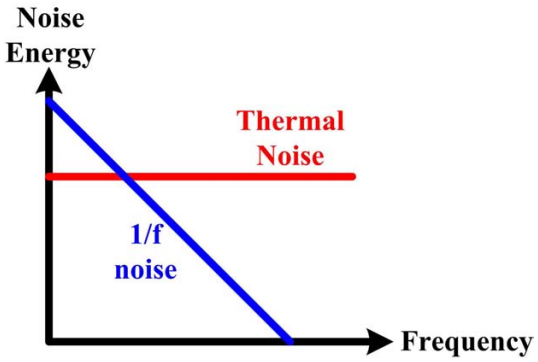

Figure 2.9: Thermal noise and flicker noise against frequency, both axis in log scales.

current dependant $1/f$ noise in CNTs resistor [9], which is regarded as a form of flicker noise. Snow, et al. also reported $1/f$ noise in 2-dimensional CNT resistors networks [39].

2.6.2 Noise in CNT Sensors Fabricated using DEP Process

Although Collins, et al. and Snow, et al. gave empirical formulas for CNT $1/f$ noise, their formulas have differences and suggest that noise modeling for CNTs may differ with the fabrication process. We performed noise measurement experiments on our CNTs sensors and found that significant flicker noise exist in our sensors.

Experimental Setup

An Audio Precision® System Two Cascade Plus audio analyzer [1] is used to analyze the noise properties of CNT sensor resistance. Its input channels have sensitivity of -160 dBV in audio frequency range (20 Hz to 20 kHz). Unfortunately, the input gain of the audio analyzer is not high enough for noise measurements and the input channels have a low input impedance ($\sim$ 50 Ω).

To remedy this problem, a preamplifier circuit is used to amplify the noise and isolate the input impedance of the audio analyzer, the schematic diagram being

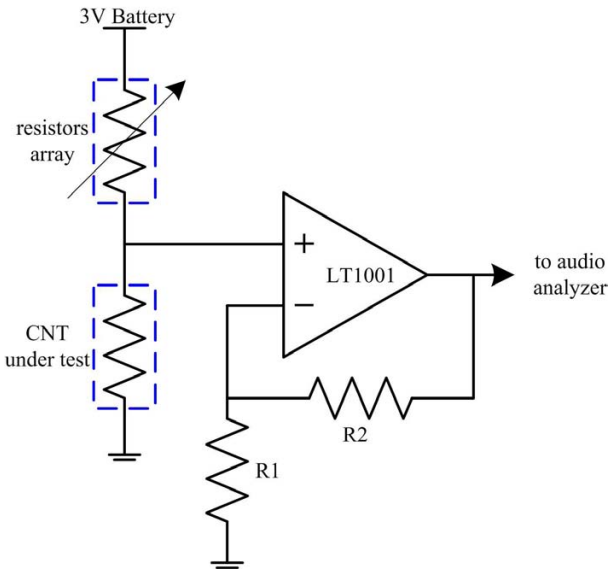

Figure 2.10: Schematic diagram of the circuit used for CNT sensor resistance noise measurement. The circuit provide variable, low noise biasing current for CNT, it also provide driving strength to drive the relative low input impedance of the audio analyzer.

shown in Fig. 2.10. An LT1001 operational amplifier [26] in the non-inverting configuration is chosen as the preamplifier because it provides a low output noise in the covered frequency range with a source impedance of a few $k\Omega$. Two metal film resistors $R1 = 51\ \Omega$ and $R2 = 1\ k\Omega$ are used to set the gain to 19.6 V/V.

A resistor array and battery are used to provide a low noise, adjustable bias current for the CNT resistor. The resistance of the array was kept large compared with the CNT resistance, hence, CNT sensor resistance dominates the resistance between AC ground and the op-amp's positive input. Noise of that input is dominated by CNT sensor resistance noise.

To minimize the noise from the environment, the CNT sensor, circuit board and the power supply (batteries) are sealed in an aluminum box to prevent environmental electric noise. The aluminum box is then sealed by mu-metal to prevent environmental magnetic noise. Before we start our experiments, the CNT sensor is replaced by a metal wire so that the background noise data is collected. This is measured ten times and the average value shown in Fig. 2.11. The noise floor

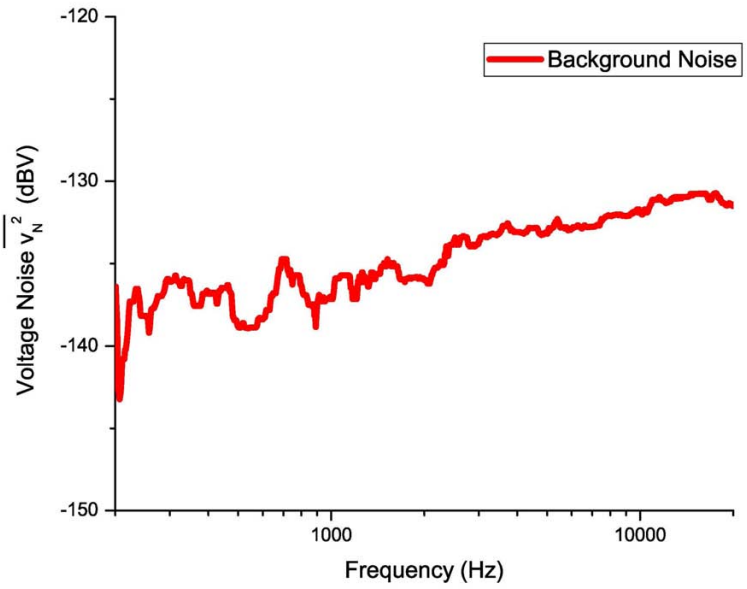

Figure 2.11: 10 Averaged background noise of our noise measurement setup.

is $\sim$ -135 dBV.

Results and Discussions

We tested two CNT sensor fabricated by DEP process. Sensor (A) (3.68 $k\Omega$) is made from MWNTs ordered commercially from Sun Nanotech Company Ltd., Beijing, China, which were prepared by chemical vapor deposition (CVD). Sensor (B) (1.38 $k\Omega$) is made from CNTs bought form Brewer Science®, which are electronic grade SWNTs and MWNTs. All the CNTs are not functionalized.

We performed 10 control measurements with the same setup using two metal film resistors with resistance 3.68 $k\Omega$ and 1.38 $k\Omega$. The result is used for background noise calibration. The averaged noise in the corresponding control measurements is subtrated from noise measured in Sensor (A) and Sensor (B). The results are shown in Fig. 2.12 and Fig. 2.13.

We tried to fit the measured results to eq. 2.2, and a summary is shown in Table 2.1. The frequency dependence is quite consistent, and we found that the

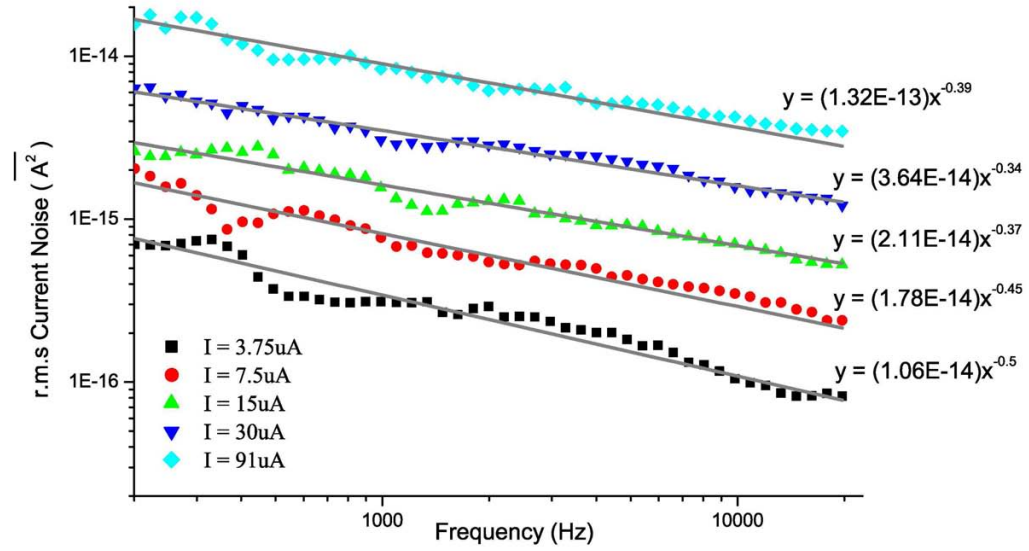

Figure 2.12: Noise measurement result for Sensor (A) (subtracted by noise of 3.68 $k\Omega$ metal film resistor) with different conducting current and the fitted curve.

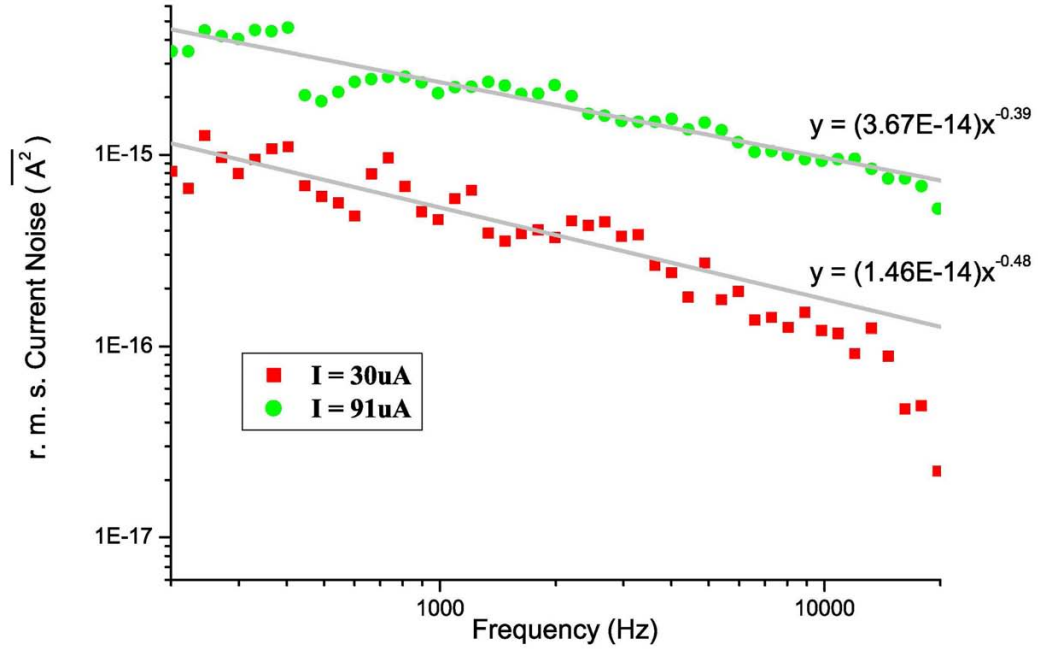

Figure 2.13: Noise measurement result for Sensor (B) (subtracted by noise of 1.38 $k\Omega$ metal film resistor) with different conducting current and the fitted curve, noise measured under 30 uA conducting current is insignificant compared with background noise.

noise is roughly proportional to ($f^{-0.45}$) where f is the frequency. However, no conclusion could be make regarding current dependence and device dependence, more experiments with different kinds of CNT sensor should be conducted.

Form the analysis, we find that CNT sensor resistance noise decreases with increasing frequency. Hence it is suggested that we should measure the CNT sensor' impedances at high frequencies rather than DC.

		device constant (K_1)	frequency dependence (b)	current dependence (a)
Sensor(A)	min	3.18×10^{-13}	-0.5	0.24
	max	6.51×10^{-9}	-0.34	1.16
Sensor(B)	min	8.35×10^{-11}	-0.48	0.83
	max	/	-0.39	/

Table 2.1: Summary parameters for CNT resistors found via curve fitting with eq. 2.2.

2.7 CNT Sensors

It has been shown that CNTs can be used as sensors for pressure, fluid-flow and alcohol [12, 14, 37]. In this section, we will give a brief introduction to the principle for each sensing application and see how the sensing condition affects our measurement technique. Fig. 2.14 shows an I-V curve of a CNT sensor. When the CNT is biased with small current, its temperature remains unchanged and the I-V curve is linear. When the CNT is biased with a larger current, its temperature rises and resistance changes due to finite temperature coefficient. This results in a non-linear I-V curve.

2.7.1 Pressure Sensors

When pressure is applied to a piezoresistor, strain will be induced and the resistance of the resistor will change. This effect is called the piezoresistive effect, and

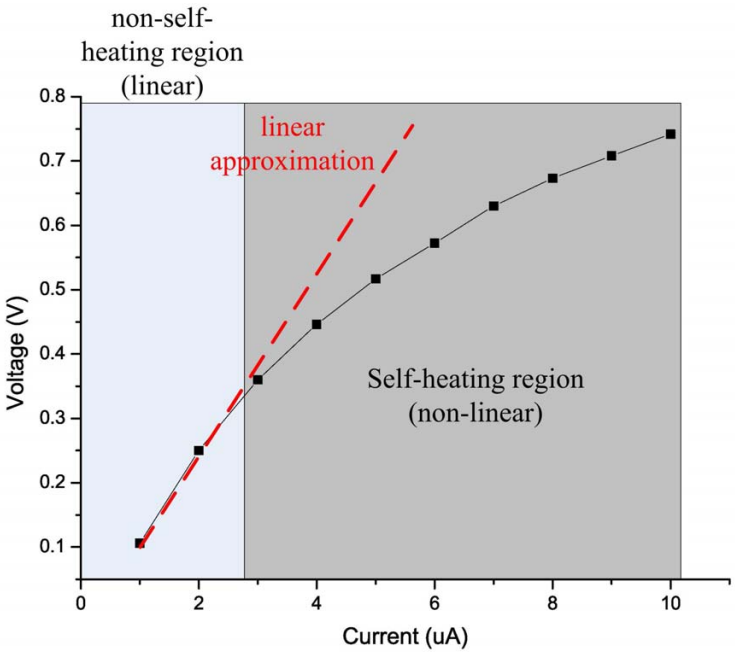

Figure 2.14: I-V curve of a CNT sensor

the characteristic of a piezoresistor can be modeled by its gauge factor (G) using eq. 2.3 [48]. A larger gauge factor corresponds to better responsivity. Silicon based piezoresistors are usually employed in electronic pressure sensors. However, Li, et al. showed that CNTs have a gauge factor of 450-800, which is ~ 4 times higher than a traditional silicon piezoresistor [16], and is hence potentially a better sensor.

$$G\varepsilon = \frac{\Delta R}{R} \tag{2.3}$$

where

G = gauge factor

ε = applied strain

ΔR = resistance change due to applied strain

R = original resistance

When CNT sensor is used as piezoresistor, we should limit the bias current to

a small value so that self-heating is minimized. The threshold value of this bias current varies from sensor to sensor, and we can determine its value from the I-V curve of the sensor (Fig. 2.14).

2.7.2 Fluid-Flow Sensors

The rate of fluid-flow around a CNT sensor affects the heat transfer between the CNT sensor and the environment. This heat transfer affects the power required to heat the CNT sensor to a specific temperature, hence, CNT sensor carefully biased for self-heating can be used for fluid-flow rate sensors [12]. CNT-based fluid-flow sensors are easily self-heated so that they have μW power consumption compared with mW power consumption of polysilicon based resistors [12]. We can also use the CNT fluid-flow sensor at a scale of hundreds of micrometers within a micro wind tunnel. Fluid-flow inside the tunnel is increased due to compression and the responsivity is increased [12].

2.7.3 Alcohol Sensors

Carbon is the fundamental building block for CNTs and chemical reactions may occur between the CNT sensor and organic molecules. Molecules may attach to the CNTs and the resistance of the CNT sensor will be altered due to the change in molecular structure. Using this mechanism we can use CNT sensor as chemical detectors [22, 37].

During alcohol detection, the CNT sensor should be biased in the non-self-heating region so that fluid flow will not affect the CNT sensor resistance. After detection, the CNT sensor may be biased into self-heating so that the attached alcohol will evaporate and detach [37].

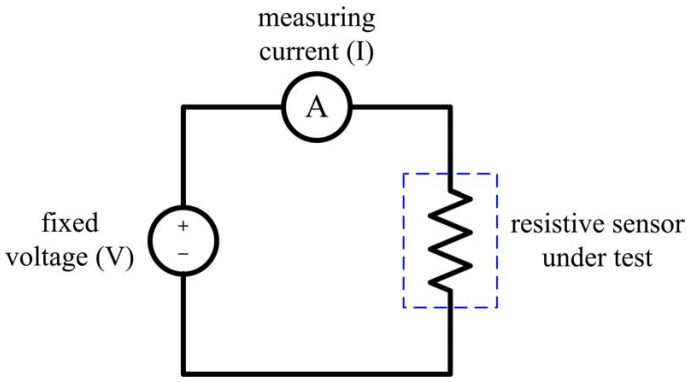

Figure 2.15: Constant voltage approach for resistive sensor response measurement.

2.8 CNT Sensor Response

Many measurement approaches can be employed for resistive sensors. Some of them measure the actual resistance change and some measure parameters in a feedback loop. Each approach has its advantages and disadvantages, and some approaches have their special role in some specific applications. In this section, we will review some of these approaches.

2.8.1 Traditional Sensor Response Measurement Techniques

Constant Voltage and Constant Current Approaches

Constant voltage (C.V.) and **constant current (C.C.)** are two simple techniques to measure resistive sensor response. Both of them target resistance change. In the C.V. approach, a fixed bias voltage is applied to the resistor. An ammeter is used to measure the resulting current and the response of the sensor (resistive change) is calculated (Fig. 2.15). In the C.C. approach, a constant current is applied to the sensor and a voltmeter is used to measure the induced voltage (Fig. 2.16). The change in resistance is then calculated. In practice, the C.C. approach is usually preferred over the C.V. approach because current measurement is more difficult compared with voltage measurement.

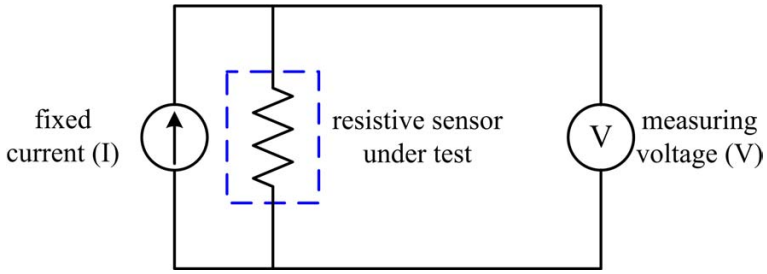

Figure 2.16: Constant current approach for resistive sensor response measurement.

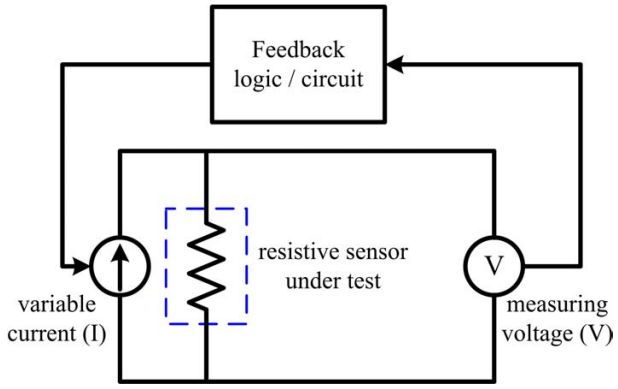

Figure 2.17: Controlled current constant power circuit, power ($P = V \times I$) is kept constant by feedback logic.

C.V. and C.C. approaches provide simple solutions for resistive sensor measurement, however, they have significant weaknesses. Firstly, they are conducted using static voltage and current, so the measurements are easily corrupted by low frequency noise in the CNT sensor, making a high signal-to-noise ratio (SNR) measurement difficult. Secondly, the power dissipated by the CNT sensor changes with applied current or voltage. This affects temperature sensitive applications such as fluid-flow sensors.

Constant Power Approach

The **constant power (C.P.)** approach is similar to C.V. and C.C. approaches, but the power dissipation of the sensor ($P = I \times V$) is kept constant through feedback. Fig 2.17 shows the controlled current C.P. approach. As both bias

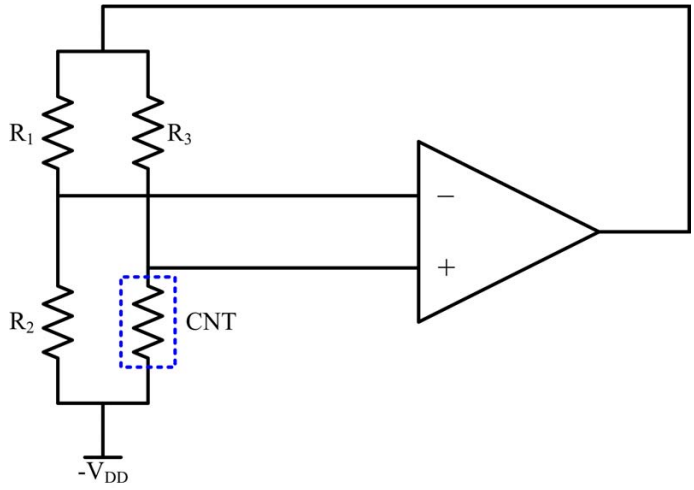

Figure 2.18: A constant temperature / constant resistance CNT response measurement circuit. The CNT sensor resistance has negative temperature coefficient and R_1, R_2 and R_3 have zero temperature coefficient. The resistance / temperature of CNT is kept constant by negative feedback.

current and voltage changes, the response becomes complex. The C.P. approach is useful in some fluid-flow applications where a constant power dissipation across the resistive sensor is necessary [27].

Constant Resistance / Constant Temperature Approach

The C.P. approach can be extended to a resistor with known monotonic temperature coefficient to keep the sensor resistance constant (i.e. the temperature of the resistor is kept constant). We call this the **constant resistance (C.R.)** or **constant temperature (C.T.)** approach. Fig. 2.18 shows an example of the C.R. approach with a negative temperature coefficient CNT sensor. Note that this technique cannot be applied to a resistive sensor with non-monotonic temperature coefficient as the feedback loop may oscillate. Similar to the C.P. approach, the measured voltage / current may have a non-linear relationship with the applied value and a mapping function may be required. The C.R. approach is found to be more useful in fluid-flow applications compared with the C.P. approach [27].

2.9 Accuracy of CNT Sensor System

The accuracy of our CNT sensor measurement can be defined by its **signal to noise ratio (SNR)** which is calculated by [45]:

$$S/N = \frac{P_{signal}}{P_{noise}} \tag{2.4}$$

where

S/N is the signal to noise ratio

P_{signal} is power density of the signal

P_{noise} is the power density of noise

In a constant current mode measurement, the voltage across the CNT sensor remains unchanged when the stimulus current is constant. Any fluctuation on the voltage across the CNT sensor is regarded as noise and the DC component of the voltage is our signal. If the voltage across the CNT sensor is sampled, we can represent the signal and noise by:

$$v_{CNT}[i] = v_{CNT\_DC} + v_{CNT\_AC}[i] \tag{2.5}$$

where

$1 \leq i \leq N$

$v_{CNT}[i]$ is the sampled voltage across the CNT sensor

v_{CNT_DC} is the DC component of $v_{CNT}[i]$ and signal of the measurement

$v_{CNT\_AC}[i]$ is the AC component of $v_{CNT}[i]$ and noise of the measurement

The DC component is defined by:

$$v_{CNT\_DC} = \frac{1}{N}\sum_{i=1}^{N} v_{CNT}[i] \tag{2.6}$$

Obviously, the power density of signal (P_{signal}) of the measurement is defined by:

$$P_{signal} = v_{CNT\_DC}^2 \tag{2.7}$$

The power density of noise (P_{noise}) in the series is defined by [31]:

$$P_{noise} = \frac{1}{N}\sum_{i=1}^{N} |v_{CNT}[i] - v_{CNT\_DC}|^2 \tag{2.8}$$

We investigated the SNR of CNT sensor measurements using a Keithley model 2400 sourcemeter [21]. The sensors are biased with a constant current and the voltage across the sensor is sampled 100 times with a 1.43 Hz sampling rate. The SNR of a 10 $k\Omega$ metal film resistor is also investigated with the same setup. The calculated SNR of 2 CNT sensors and the resistor are shown in Table 2.2.

Device under test	SNR (dB)	Resistance ($k\Omega$)
Sensor 1	75.2	9.6
Sensor 2	61.6	3.63
10 $k\Omega$ resistor	85.9	10

Table 2.2: Signal to noise ratio in CNT sensor and metal film resistor measured by Keithley model 2400 sourcemeter.

Our investigation showed that CNT sensor measurement SNR is restricted to $\sim$ 61-75 dB by its intrinsic noise (noise contributed by CNT sensor itself rather than the measuring system). One possible noise source is the frequency dependent noise we measure and explain in section 2.6.2.

2.10 Summary

In this chapter, we reviewed CNT devices, and demonstrated difficulties in using individual CNT as sensor. The DEP fabrication process solves these difficulties. We also introduced noise theory in traditional resistors and the measured noise in our CNT sensor. The working principles of CNT sensors and their response

measurement techniques are also given in the chapter. Finally, we introduced the SNR as a figure of merit for sensor accuracy.

Chapter 3

Design and Analysis of a CNT-CMOS Integrated Sensor

3.1 Introduction

The simplicity of DEP-based CNT sensor fabrication provides an opportunity to integrate a CNT sensor with a commercial CMOS process. In this chapter, such an integrated sensor will be presented.

We start the chapter by introducing the idea of CNT-CMOS integration, the reasons that special analog circuitry is needed for CNT sensors and the advantages of integration. Then, we define the goals of our CNT-CMOS prototype and its architecture. The detailed design and analysis of the 3 major components in the prototype, including the programmable current source, the ADC and the electrodes for CNT sensor are then given.

We also present the problems related to CNT electrodes, including issue created by passivation layer and the problem of aluminium oxidation. New electrodes that address this issue along with a chemical gold plating process to solve the oxidation problem are given. We believe that togethers, these solve key problems for integrating CNT sensors in commercial CMOS processes.

In the final section, we proposed an integrated alcohol sensor using an FPGA board for the digital control. This demonstrates the first integration of CNT

sensors on a CMOS IC using DEP process.

3.2 Introduction to CNT-CMOS Integration

3.2.1 Difficulties with Commercial CNT Sensors

From the review given in chapter 2, we recall that requirements for DEP-based CNT sensor fabrication include CNTs (buffered in a buffer solution), an electrode pair with small gap separation ($\sim$ tens of um) and an AC voltage. Electrodes of this type are difficult to fabricate and require a precise photolithographic fabrication process.

Owing to its small dimensions, a CNT sensor is easily self-heated so a small bias current should be used for resistance measurement. However, some applications require self-heated CNT sensors with a significantly higher signal voltage. As a result, either a variable gain stage or a high resolution ADC should be used to maintain a reasonable SNR in measurement and prevent overflows.

3.2.2 Novel Idea for CNT-CMOS Integration

Li and Leong [32] proposed a new methodology for integrating CNT sensors using CMOS technology, the idea being illustrated in Fig. 3.1. The top layer metal in the CMOS chip is designed to act as the electrodes for CNT sensor fabrication. Openings in the passivation layer are made to expose the electrodes, and CNTs may be attached using DEP force. The CMOS transistors, resistors and capacitors in the lower layers are used for CNT resistance measurement. The metal layers between the active elements layers and top metal connect them and a single chip, compact sensor can be made.

The advantages of this CNT-CMOS integration are as follows:

- By using CMOS IC, the size of the whole sensor system can be reduced to few mm^2. It may be applied to applications that were not possible in the

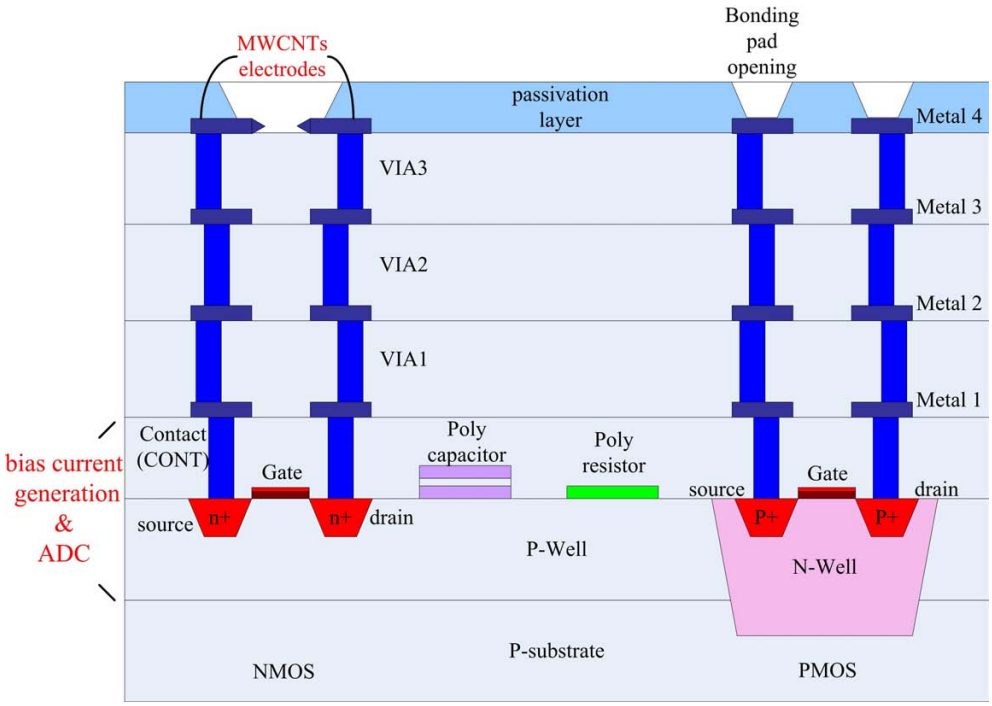

Figure 3.1: Cross-sectional area of CNT-CMOS integration.

past, for example, micro-fluidic flow measurement [12].

- Bulky equipment is no longer necessary for resistance measurement, hence, cost for ownership and power consumption is reduced. It is estimated the cost of each CNT-CMOS IC is lower than a few USD.

- The CNT sensor electrodes are fabricated using a commercial CMOS process. This achieves the required resolution with no additional cost.

3.3 Design and Analysis of a CNT-CMOS Sensor Prototype

3.3.1 Goals of CNT-CMOS Integrated Sensor

To demonstrate the feasibility of CNT-CMOS integration, we constructed a CMOS prototype chip. Due to the limitations in time and fabrication cost, we limit the

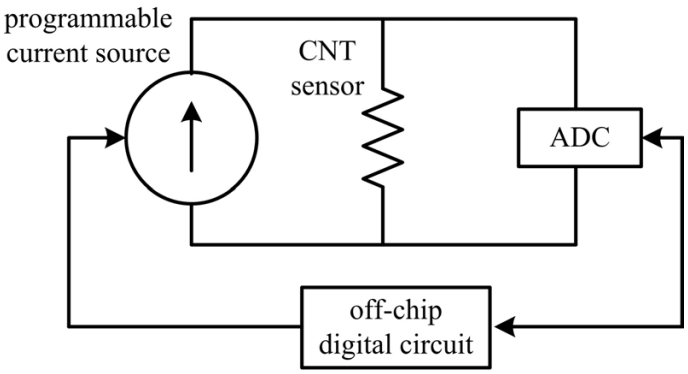

Figure 3.2: System architecture of CNT-CMOS prototype.

goals to the following:

- Demonstrating the feasibility of CNT-CMOS integration is the major goal of our prototype.
- A design with simple architecture and minimal on-chip components so that fabrication cost and design time are reduced.
- Digital control circuits, some passive components and some voltage reference circuits can be off-chip to reduce fabrication cost.

Although the prototype requires some off-chip components, it is sufficient to show the feasibility of CNT-CMOS integration. The design could be improved for a commercial product.

We chose the Austriamicrosystems® (AMS) C35B4M3 process to fabricate our prototype [7]. It is a 0.35 micron CMOS mixed-signal process with 3.3 V and 5 V transistors. Our design can be translated to other mixed-signal CMOS processes.

3.3.2 Architecture of CNT-CMOS Sensor

As a first design, we decided to use the constant current approach for sensor measurement. A constant power approach can be implemented with the same

analog hardware and a different digital circuit. The simplified system architecture of the prototype is shown in Fig. 3.2. A programmable current source is used to provide constant current for the CNT sensor, an analogue to digital converter (ADC) is used to read the voltage across CNT and an off-chip digital circuit is used for controlling the current source and ADC. By using an off-chip digital circuit, we can reduce the die area of the prototype and the complexity of testing. It can be replaced by an on-chip digital control in a later design.

From the analysis in the previous chapter, we found that the maximum achievable SNR in a DC resistance measurement is $\sim 60\ dB$, and the maximum and minimum voltage in all CNT sensor applications are $\sim 2\ V$ and $\sim 0.2\ V$ respectively. Hence, we require a 13-bit ADC with input range 0-2.42 V for a 10-bit ($\sim 60\ dB$) measurement at 0.2 V. The maximum input range is set to 2.42 V because it is 2 times a traditional bandgap voltage reference and easy to obtain.

3.3.3 Programmable Current Source

Specifications of Programmable Current source

The current source should be programmable for two reasons, firstly, different applications require different self-heating and bias current. Secondly, the resistance of CNT sensors are not well controlled in fabrication, so a programmable current source is thus necessary to keep voltage across the CNT fairly constant under this variation. Based on the experimental results of our group, the minimum and maximum current should be 2 uA and 400 uA respectively, hence, we decided to make the current source programmable from 0 uA to 510 uA in 2 uA steps.

Temperature dependance of current directly affects the measured resistance. The relation between required accuracy of measurement, temperature coefficient of current and range of working temperature is stated in Eq. 3.1 [29]. For example, if the prototype is used with a 20 ℃ temperature variation and a 60 dB accuracy is required, the temperature coefficient of the current source should not

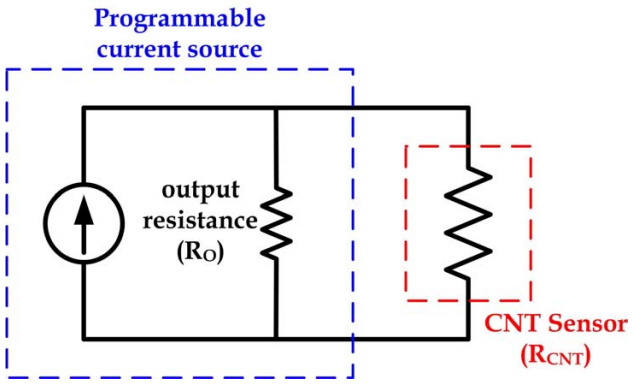

Figure 3.3: Output resistance of programmable current source.

exceed $1/(10^{60/20} \times 20) = 50\ ppm$ (parts per million).

$$T_C \times T_V < \frac{1}{10^{SNR/20}} \tag{3.1}$$

where

T_C = Temperature coefficient of current source

T_V = Working temperature range of the IC

SNR = Required measuring accuracy in dB

Output resistance (R_O) of the current source affects the measurement accuracy as illustrated in Fig. 3.3. R_O should be kept high relative to the resistance of the CNT sensor (R_{CNT}). Although CNT sensor resistance may as high as several $k\Omega$, the current source output resistance is not a problem in our prototype.

Output current noise is another current source parameter that affects our measurement accuracy. As the noise is directly coupled into the CNT sensor, we have to keep it small. Fortunately, we can ignore the high frequency noise when we are measuring the CNT sensor resistance using DC methods.

Architecture of Programmable Current Source

Fig. 3.4 shows the architecture of our programmable current source. A reference current (I_{REF}, $\sim 2\ uA$) is made by applying a reference voltage from a bandgap

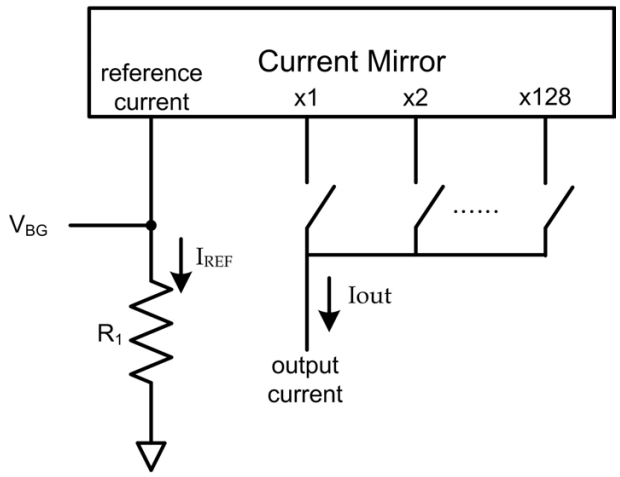

Figure 3.4: Simplified architecture of programmable current source.

(V_{BG}) to a V-I converter (Voltage to Current Converter) and the resulting current is equal to V_{BG}/R_1. The reference current is then duplicated via binary weighted current mirrors in which 8 switches are used to control each current mirror. Hence the output current (I_{OUT}) is switchable from 0 uA to 510 uA in 2 uA steps.

Two CMOS resistor non-idealities affect our reference current construction. Firstly, the absolute value of fabricated CMOS resistors exhibit a variation of (+/- 20%) due to random errors of etching and impurity doping level in fabrication [17]. Secondly, CMOS resistors have finite temperature coefficient and hence introduce temperature dependance into the reference current. We can reduce both non-idealities via trimming, however, it is time consuming and expensive.

In sensor applications, we are mainly interested in the relative change in resistance ($\Delta R/R_{initial}$) rather than the absolute resistance change (ΔR). The absolute value of the reference current affects measurement in absolute resistance change but not relative resistance change.

The temperature coefficient of the reference voltage (V_{BG}) is designed to match the temperature coefficient of the CMOS resistor (R_1). The resulting reference current will, to a first order, have zero temperature coefficient.

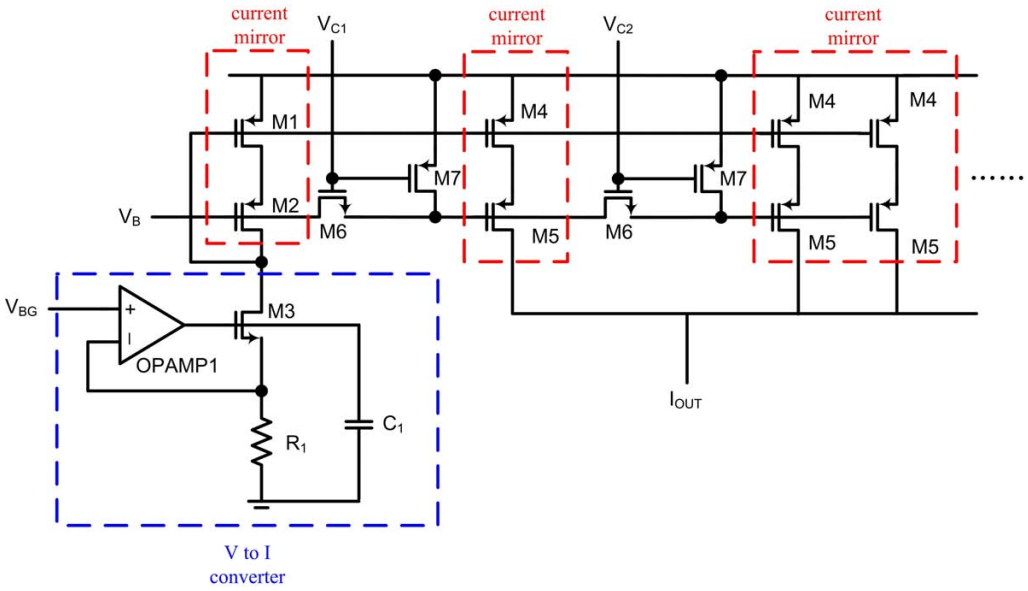

Figure 3.5: Schematic of programmable current source, parameters are shown in Table 3.1

Transistor	M1	M2	M3	M4	M5	M6	M7
Sizing(um)	16/12	5/0.5	10/0.5	16/12	5/0.5	2/0.5	2/0.5
Component	R_1	C_1					
Value	$467k\Omega$	$10.8pF$					

Table 3.1: Parameters of components of programmable current source.

Implementation of Programmable Current Source

The schematic and parameters for the programmable source is shown in Fig. 3.5 and Table 3.1 respectively. Transistors M1, M2, M4 and M5 form the current mirrors. The base transistors (M1, M4) are made significantly larger than minimum size to improve matching. As the $1/f$ noise of current mirror is inversely proportional to the gate area ($W \times L$) of the base transistors [15], their large size also reduces $1/f$ noise from the current mirror. The cascode transistors (M2, M5) do not significantly contribute to the output noise and mismatch of the current mirror, hence they are made with much smaller channel length (0.5 um). The transistors are biased so that the saturation voltage ($vdsat$) of the base transistors (M1, M4) are $\sim 300\ mV$, hence, the temperature dependance of the current mirrors are better matched, and the saturation voltage of the cascode transistors are much smaller ($\sim 100\ mV$) to preserve voltage headroom.

The current mirrors are controlled by a set of control voltages ($V_{C[1,2,4...128]}$) through two transistors (M6 & M7). When $V_{C[X]}$ is high, M6 will be turned on and M7 will turned off, thus the corresponding current mirror will contribute X times the reference current. When the control voltage is low, M6 will be turned off and M7 will turned on, the cascode transistor M5 is thus tied to V_{DD} and hence the corresponding current mirror is turned off.

A single stage folded cascode operational amplifier (OPAMP1), a high resistance poly resistor and a modified bandgap voltage reference (V_{BG}) form a V to I converter. We use a single stage folded cascode op-amp (Fig. 3.6) because it provides excellent frequency response and the DC gain is high enough for our application. A poly-poly capacitor (C_1) is used to decrease the unit gain frequency (UGF) so that high frequency noise from the bandgap voltage reference is not coupled into the output current.

In the AMS C35B4M3 fabrication process, the temperature coefficient of a high resistance poly resistor is -650 $ppm/$°C. We have to design a bandgap voltage

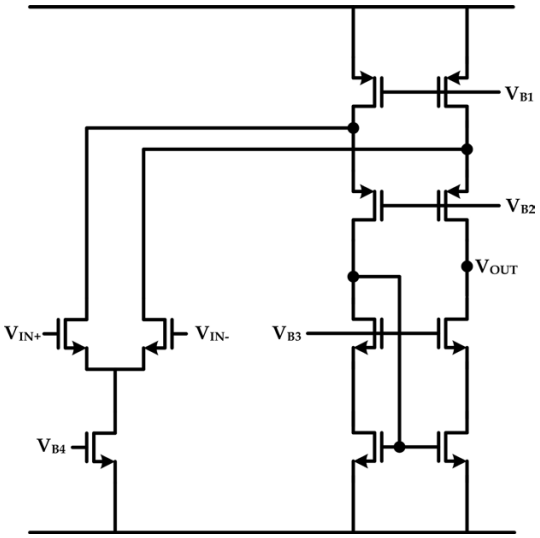

Figure 3.6: Single stage folded cascode op-amp used in V to I converter.

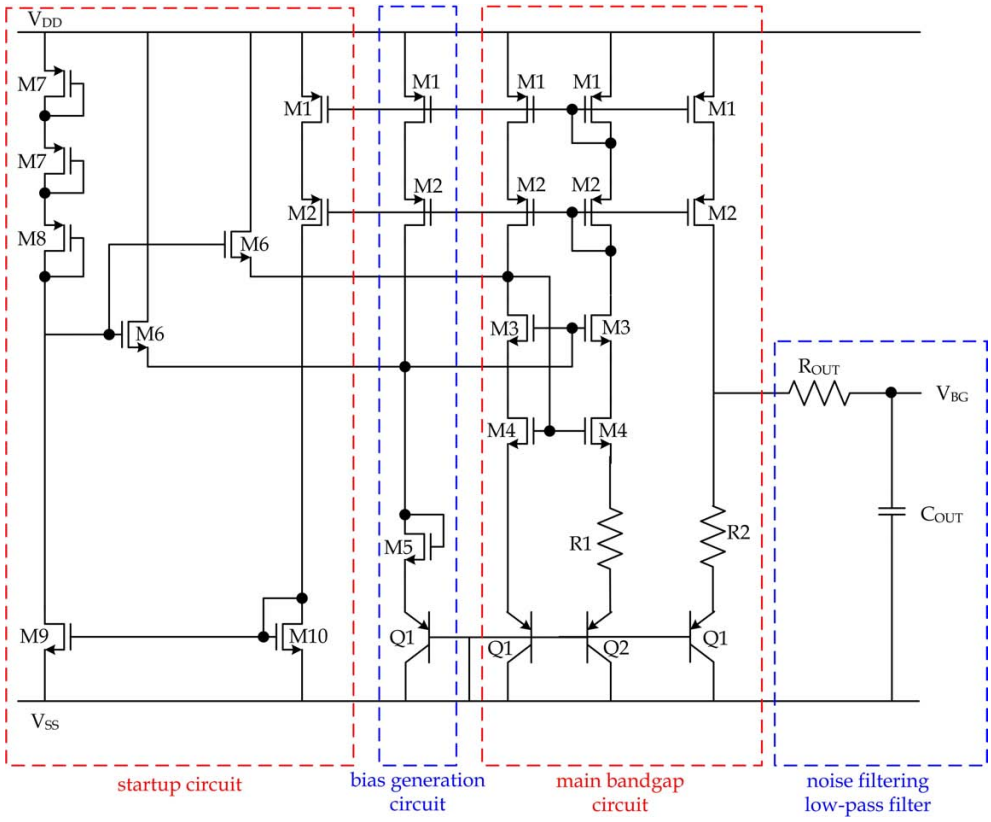

Figure 3.7: Cascode current mirror bandgap voltage reference used in our programmable current source.

Transistor	M1	M2	M3	M4	M5
Sizing(um)	15/12	4/1	8/32	1.5/40	5/2.5
Transistor	M6	M7	M8	M9	M10
Sizing(um)	5/2.5	5/5	1/30	1.5/40	1/3
Component	R_1	R_2	$Q_1 : Q_2$	R_{OUT}	C_{OUT}
Parameter	$26k\Omega$	$174.5k\Omega$	1:8	$1M\Omega$	$20.8pF$

Table 3.2: Parameters of bandgap voltage reference.

reference with a temperature coefficient of -650 $ppm/$℃ so that the ratio (V_{BG}/R_1) is independent of temperature and the temperature coefficient of the V to I converter is zero to a first order. As the supply voltage of our IC is 5 V and we have enough voltage headroom for cascoding, a cascode current mirror bandgap voltage reference was selected [15]. The implementation is shown in Fig. 3.7 and the parameters are shown in Table 3.2. A startup circuit is added to bring the circuit to a correct operating point and an RC filter is added to filter out high frequency noise from the output. The output voltage (V_{BG}) of the bandgap voltage reference can be calculated from Eq. 3.2 [25, 40].

$$V_{BG} = V_{BE} + [(\frac{R_2}{R_1})ln(N)]V_T \tag{3.2}$$

where

V_{BE} is the emitter-base voltage of bipolar transistor Q_1

N is the ratio $Q_2 : Q_1$

V_T is the thermal voltage, represented by:

$$V_T = \frac{kT}{q} \tag{3.3}$$

where

k is Boltzmann's constant

T is temperature in (K)

Q_2	Q_2	Q_2
Q_2	Q_1	Q_2
Q_2	Q_2	Q_2

Figure 3.8: Illustration of 3×3 layout matrix for 8:1 bipolar transistor matching.

q is the charge of an electron

V_T equal to 26 mV at $T = 300$ K and has a positive temperature coefficient of 0.0862 mV/℃.

V_{BE} is represented by [25, 40]:

$$V_{BE} = V_G(T_o) + \frac{T}{T_o} \cdot [V_{BE}(T_o) - V_G(T_o)] - (\eta - m)\frac{kT}{q} ln(\frac{T}{T_o}) \tag{3.4}$$

where

V_G is the bandgap voltage of silicon

η is the temperature constant which is dependent on technology

m is the order of the temperature dependence of the collector current

T_o is the reference temperature

From the process parameters of the AMS® C35B4M3 process, V_{BE} is $\sim$ 0.7 V and has a temperature coefficient equal to $\sim$ -2 mV/℃.

From Eq. 3.2 we found that the temperature coefficient of the bandgap voltage reference can be adjusted by the ratio R_2/R_1 and $Q2/Q1$. The lower limit of this temperature coefficient is $\sim$ -2 mV/℃. We designed the bipolar transistor ratio to be 8:1 so it can laid out in a 3×3 matrix (Fig. 3.8). This layout is compact and Q_1 and Q_2 have a common centroid. This helps to match the transistors as it has minimal area and symmetrical layout [17].

Simulation Results and Layout of Programmable Current Source

Parametric simulations on the R_2:R_1 were ran to obtain a -650 ppm/℃ temperature coefficient for V_{BG}. We found the ratio should be 6.7115:1 (174.5 $k\Omega$: 26

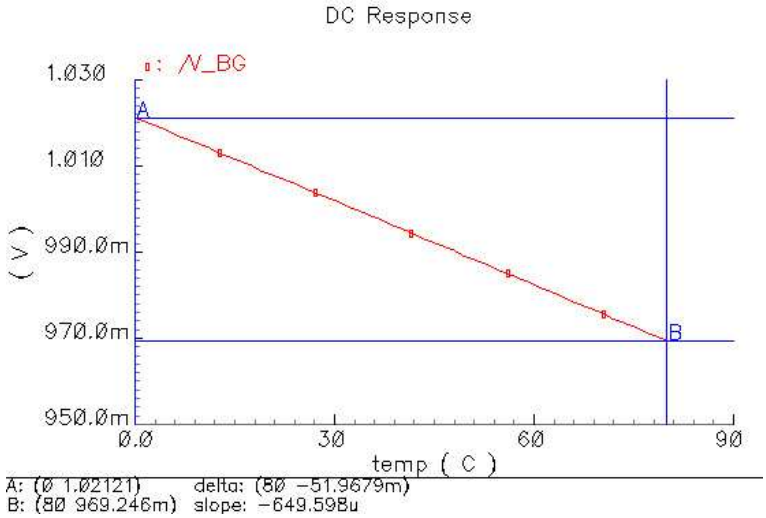

Figure 3.9: Simulated temperature dependance of modified bandgap voltage reference in 0 ℃ to 80 ℃, the output voltage is $\sim 1\ V$ and the temperature coefficient is $-650\ ppm/$℃.

$k\Omega$). Fig 3.9 show the simulated temperature coefficient of the modified bandgap voltage reference.

The temperature coefficient of the whole programmable current source is then simulated for two extreme cases, **I)** $I_{OUT} = 2\ uA$, **II)** $I_{OUT} = 510\ uA$, V_{OUT} is set to $1\ V$ in both cases (Fig. 3.10) and the temperature is swept from 0 ℃ to 80 ℃ to obtain Fig. 3.11 and Fig. 3.12 respectively. Both cases show a 80 $ppm/$℃ temperature coefficient due higher order mismatch between the bandgap voltage

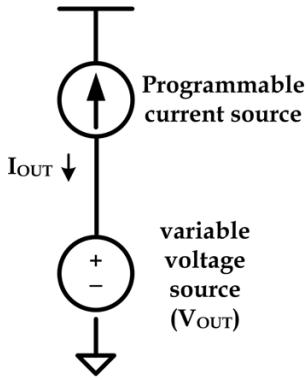

Figure 3.10: Simulation setup for programmable current source.

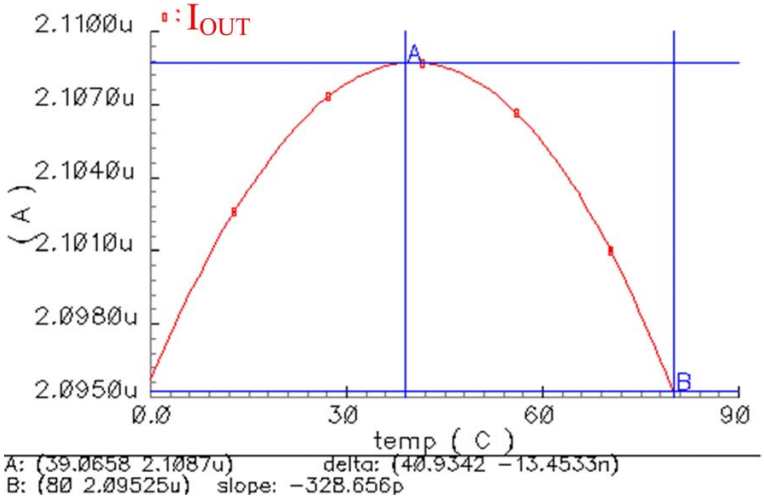

Figure 3.11: Temperature dependance of programmable source at output=2.1 uA.

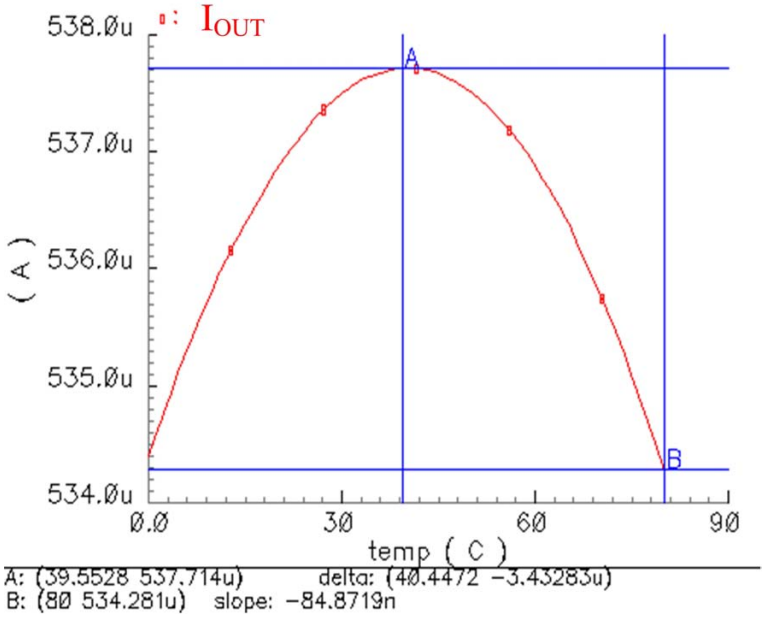

Figure 3.12: Temperature dependance of programmable source at output=536 uA.

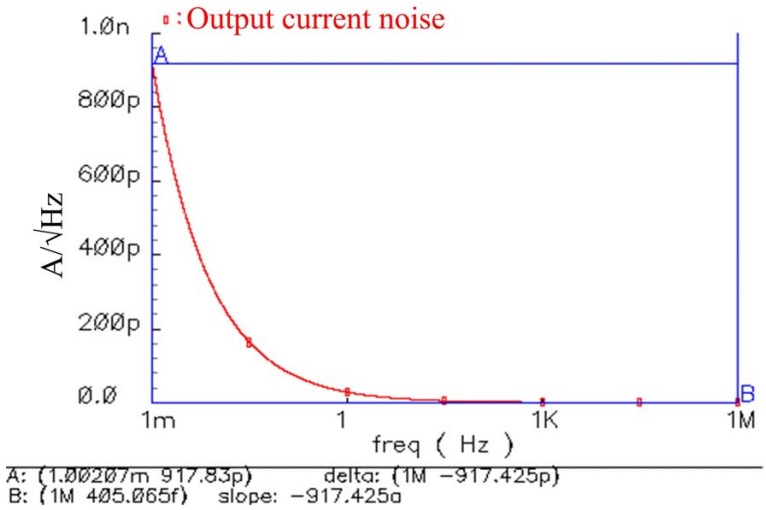

Figure 3.13: Output current noise of programmable current source.

reference and high resistance poly resistor. It is expected that the fabricated programmable source will have a larger temperature coefficient due to device mismatch which was not modeled.

The output noise current of the programmable current source is simulated from 0 Hz to 1 MHz (Fig. 3.13). Due to the large gate sizing of base transistors in the bandgap voltage reference and current mirrors, the total output noise current is 103 pA^2 (0 Hz to 200 Hz) and 439.3 pA^2 (0 Hz to 1 MHz) at an output of 2 uA. This is equivalent to a 85.7 dB and a 73.1 dB SNR. From the noise simulation, we conclude that the programmable current source is able to provide bias current for a 14-bit CNT resistance measurement using DC methods.

The output resistance of the current source at $I_{OUT} = 2\ uA$ is simulated by sweeping V_{OUT} from 0 to 2.2 V as illustrated in Fig. 3.10, the simulated result is shown in Fig. 3.14. It is showed that from the simulation result the current source have a output resistance equal (2.2 V / 7 $nA = \sim 0.3\ M\Omega$).

The programmable current source layout is done carefully, R_1, R_2 and all the other devices require good matching and are laid out following the general matching rules from reference [17]. The layout is shown in Fig. 3.15.

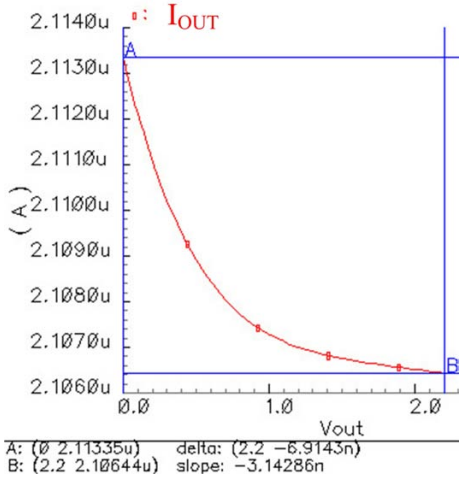

Figure 3.14: Simulated output resistance of programmable current source.

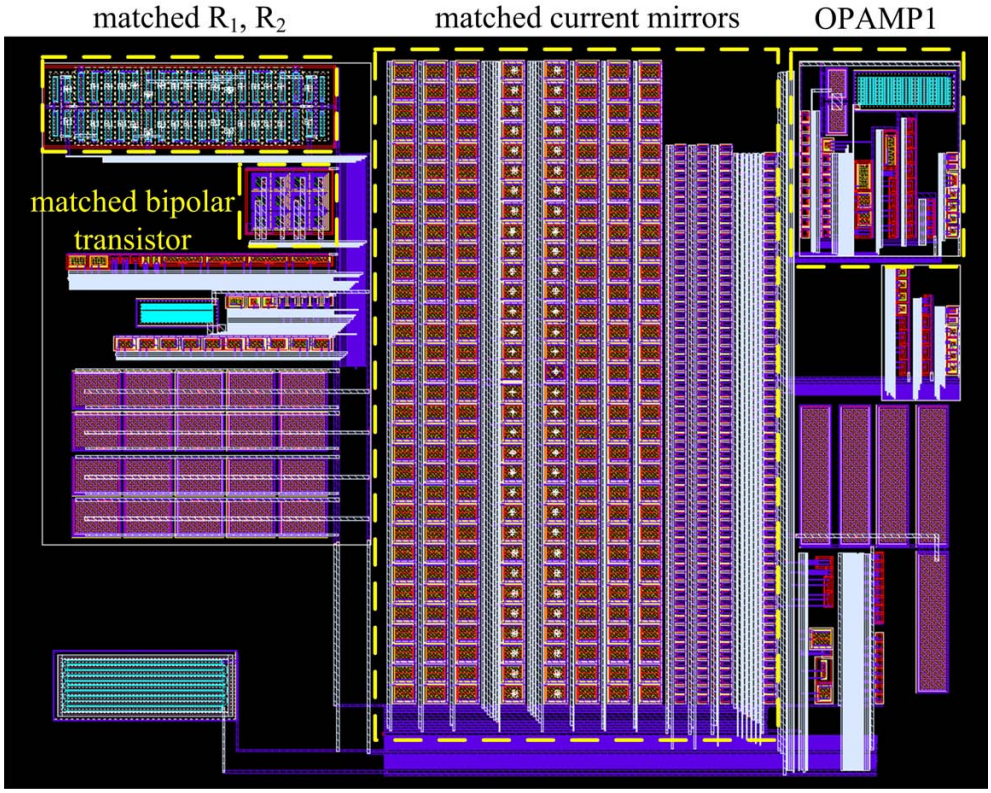

Figure 3.15: Layout of programmable current source

3.3.4 Dual Slope ADC

Choice of Architecture

Input Range	0 V - 2.42 V
Resolution	13-bit
Sampling Rate	Not Important
Chip Area	Small
Power Consumption	Low

Table 3.3: Requirements of ADC

Based on our analysis in pervious sections, we need an ADC for voltage measurement with the requirements shown in Table 3.3. The input range (0 V - 2.4 V) is defined by the maximum voltage across the CNT sensor, which is $\sim$ 2 V for the self-heating mode of operation. The resolution of the ADC is designed so that the **signal to quantization noise ratio (SNQR)** is comparable to the SNR of the CNT sensor measurement in Table 2.2.

The quantization noise power is defined by [4]:

$$E\{e^2\} = \frac{\Delta^2}{12} \tag{3.5}$$

where

$E\{e^2\}$ is quantization noise power

Δ is one quantization step, which is equal to $F_s/2^B$

F_s is the full scale input range of the ADC

B is number of bit of the ADC

The minimum voltage across the CNT sensor is $\sim$ 200 mV (non-self-heating mode). Hence, we need an ADC with 13-bit resolution so that a 67.5 dB SNQR is achieved. As we are only interested in demonstrating DC measurement with the prototype, we do not have any sampling rate requirement. Finally, we would

like to keep the chip area and power consumption low to reduce fabrication and system operating costs.

In CMOS technology, the best matching accuracy of resistors, capacitors and current source are reported to be 0.02 % - 0.1 % [17], so the maximum effective number of bit (ENOB) of an ADC in CMOS technology without calibration circuit or other special circuit techniques is restricted to 10 - 12 bits [35]. Two ADC architectures can achieve more than 10-bits accuracy without calibration, they are the dual slope ADC and the delta sigma ADC [44].

A dual slope ADC consists of 3 major components, an integrator (constructed from an op-amp, capacitor and resistor), comparator and counting digital logic. During each conversion, the integrator will first integrate the input signal for a fixed duration. Then it is connected to a negative reference for de-integration. The time require for de-integration is proportional to the amplitude of input voltage and is counted using digital logic [44].

Delta sigma ADCs use a low resolution quantizer (usually a single bit comparator) for input signal quantization, and the matching accuracy requirement of current source, capacitors and resistors in the quantizer is relaxed compared with high resolution ones. The sampling rate of a delta sigma ADC is much higher than the Nyquist rate and noise shaping feedback techniques are employed to reduce the quantization noise introduced by the quantizer. A low-pass digital filter, called a decimator is used to down-sample the output from the noise shaper to the Nyquist rate [19]. Hence, delta sigma ADCs can achieve high resolution even with poorly matched components.

Both dual slope and delta sigma ADCs can achieve our 13-bits accuracy requirement, however, the dual slope ADC has a simpler architecture and much smaller digital circuit, so it is chosen as our ADC architecture to reduce the design time and risk. One drawback of using a dual slope ADC is the sampling rate is restricted to 100 - 200 Hz. This is not a problem as we are interested in DC measurements only.

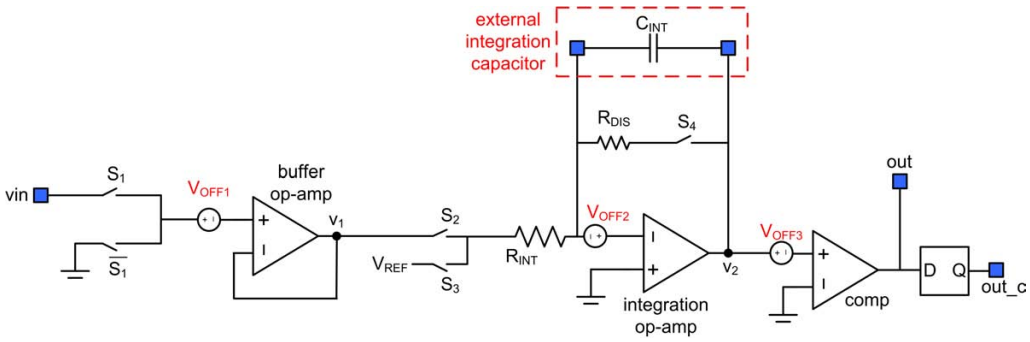

Figure 3.16: Schematic diagram for the dual slope ADC.

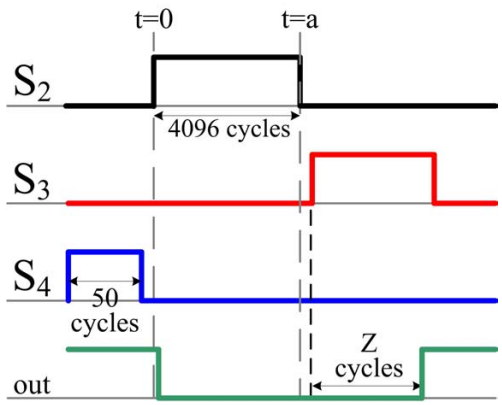

Figure 3.17: Control signals for the dual slope ADC.

Architecture and operation of Dual Slope ADC

The schematic diagram and the offset voltage of each op-amp / comparator for our dual slope ADC is shown in Fig. 3.16. The ADC is powered by a 5 V supply and the analog ground is set to be 2 V above the negative supply (V_{SS}). A buffer op-amp is used increase the input impedance of the ADC relative to the resistance of CNT sensor. It also introduces an offset voltage (V_{OFF1}) so that v_1 is equal to ($v_{IN} - V_{OFF1}$) when S_1 is high and ($-V_{OFF1}$) when S_1 is low. V_{OFF2} and V_{OFF3} are the offset voltage of the integration op-amp and comparator respectively. V_{REF} is a reference voltage which is -1.21 V (1 times a bandgap) relative to analog ground. In our analysis, the "ON resistance" of all MOS switches are assumed to be zero and the "OFF resistance" assumed to be infinity.

The ADC control signals are shown in Fig. 3.17. The master clock of the

ADC is chosen to be 204.8 kHz so that the integration time for input signal (duration of that S_1 is closed) is one period of 50 Hz. Hence, the 50 Hz signal exist in v_{IN} coupled from electricity do not affect the conversion [44]. Before each voltage conversion ($t < 0$), S_4 is turned off for 50 cycles to discharge C_{INT}, at ($t = 0$), S_4 is turned off and S_2 is turned on. Hence, a current (i_{INT}) will enter the integration capacitor (C_{INT}) and its amplitude is:

$$i_{INT} = \frac{(v_{IN} - V_{OFF1}) - (-V_{OFF2})}{R_{INT}} \tag{3.6}$$

S_2 will be turned on for a fixed duration (4096 cycles), and then S_2 will be turned off at ($t = a$). v_3 is calculated by the following equation at that moment:

$$v_3|_{t=t_a} = -[V_{OFF2} + \frac{(v_{IN} - V_{OFF1} + V_{OFF2}) \times T \times 4096}{R_{INT} \times C_{INT}}] \tag{3.7}$$

where T = one period of the master clock

S_3 is then turned on and a current (i_{DE-INT}) will flow out of C_{INT} with amplitude:

$$i_{DE-INT} = -[\frac{V_{OFF2} + V_{REF}}{R_{INT}}] \tag{3.8}$$

Y cycles later ($t = t_a$), v_3 is equal to:

$$v_3|_{t=t_b} = -[V_{OFF2} + \frac{(v_{IN} - V_{OFF1} + V_{OFF2}) \times T \times 4096}{R_{INT} \times C_{INT}}] - [\frac{(V_{OFF2} + V_{REF}) \times T \times Y}{R_{INT} \times C_{INT}}] \tag{3.9}$$

Z cycles after S_3 is turned on, comparator (out) output will become positive, and Z is equal to:

$$Z = \frac{(V_{OFF2} + V_{OFF3}) \times R_{INT} \times C_{INT}}{T \times (1.21 - V_{OFF2})} + \frac{(v_{IN} - V_{OFF1} + V_{OFF2}) \times 4096}{1.21 - V_{OFF2}} \quad (3.10)$$

If the op-amps and comparator have zero offset voltage (i.e. $V_{OFF1} = V_{OFF2} = V_{OFF3} = 0$), Eq. 3.10 reduces to:

$$Z = \frac{v_{IN} \times 4096}{1.21} \quad (3.11)$$

The problem of offset voltage can be solved by means of double sampling. Every time the chip is turned on, S_1 is made low and a conversion is started. The calibration count (Z_o) can be obtained in this conversion and it is equal to:

$$Z_o = \frac{(V_{OFF2} + V_{OFF3}) \times R_{INT} \times C_{INT}}{T \times (1.21 - V_{OFF2})} + \frac{(-V_{OFF1} + V_{OFF2}) \times 4096}{1.21 - V_{OFF2}} \quad (3.12)$$

S_1 is then turned high for normal operation. For each conversion, we subtract Z by Z_o, hence the output becomes:

$$Z - Z_o = \frac{v_{IN} \times 4096}{1.21 - V_{OFF2}} \quad (3.13)$$

From Eq. 3.13 we see that only the offset voltage of the integration op-amp (V_{OFF2}) affects our measurement, and cause a scaling error which does not affect our relative resistance change measurement.

We have to ensure the calibration count (Z_o) is positive so that we can execute the calibration. From Eq. 3.12 we found that the following conditions have to be satisfied so that Z_o will be larger than 0.

$$\begin{cases} V_{OFF2} + V_{OFF3} > 0 \\ V_{OFF2} - V_{OFF1} > 0 \end{cases} \quad (3.14)$$

CMOS op-amp and comparator have random offset voltage from -10 mV to 10 mV [15]. We intentionally introduce a +30 mV offset voltage to the integration op-amp so that Eq. 3.14 is satisfied for all conditions.

The minimum output of the integration op-amp can be calculated from the following equation:

$$min(v_2) \simeq -\frac{2.42 \times T \times 4096}{R_{INT} \times C_{INT}} \tag{3.15}$$

The output swing of our integration op-amp is $-1.5\ V < v_2 < 2.5\ V$ (relative to A_{GND}). Hence, we decided to use $R_{INT} = 1\ M\Omega$ and $C_{INT} = 50\ nF$, so $min(v_2)$ will be equal to $\sim$ -1 V.

Buffer Operational Amplifier and Integration Amplifier

A two stage Miller compensated op-amp is used as buffer op-amp. An NMOS differential pair is used because the input voltage is in the range of 2 V to 4.42 V (0 - 2 V relative to A_{GND}). A folded cascode architecture is employed in the first stage to increase the DC gain, and a source follower is used as a level-shifter to connect the first stage and second stages. A compensation capacitor is added for pole-splitting so that the op-amp has a better phase margin. The schematic and parameters are shown in Fig. 3.18 and Table 3.4 respectively.

Transistor	M1	M2	M3	M4	M5
Sizing (um)	10/3.5	5/1	1.5/1.5	2/7	10/4
Transistor	M6	M7	M8	M9	
Sizing (um)	4/7	10/0.5	100/1	28/7	
Component	C_C				
Parameter	2.6 pF				

Table 3.4: Parameters of buffer op-amp.

The integration resistor (R_{INT}) is made on-chip, hence, the capacitive load (C_{LOAD}) of the buffer op-amp should be low. The frequency response of the buffer op-amp is simulated for 0 pF and 1 pF loads. The results are summarized

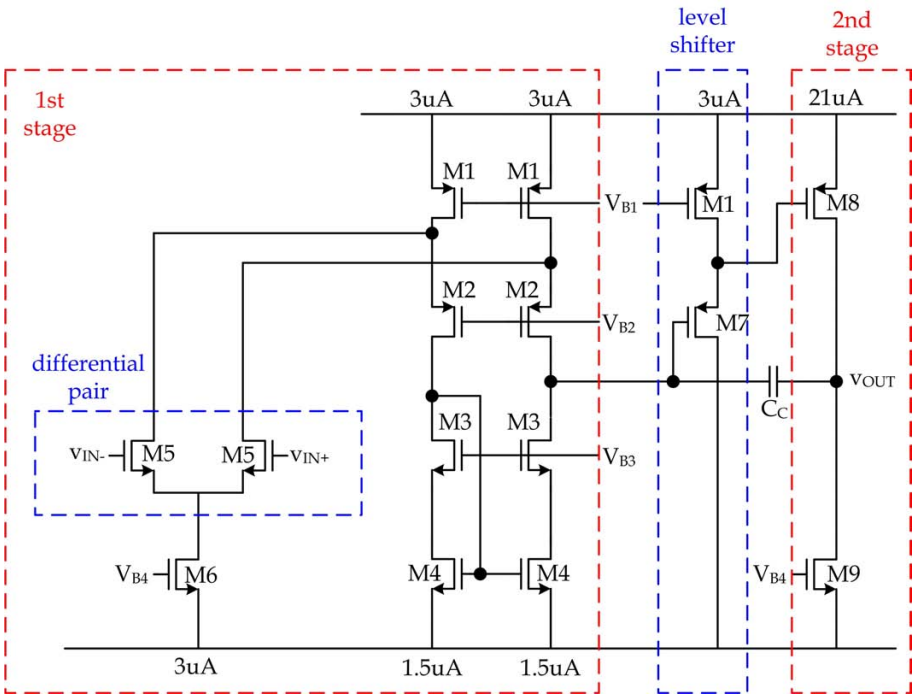

Figure 3.18: Schematic diagram of buffer op-amp.

in Table 3.5 and show that the buffer op-amp is stable and fast enough for our application.

C_{LOAD}	0 pF	1 pF
Unit Gain Frequency (UGF)	1.241 MHz	1.241 MHz
Phase Margin	82.96^o	81.27^o
DC Gain	135.7 dB	135.7 dB

Table 3.5: Frequency response of buffer op-amp.

The integration op-amp shares the same architecture with the buffer op-amp, however, its load (C_{LOAD}) is much higher due to the parasitic capacitance introduced by the leads of the off-chip integration capacitor and PCB trace. This load is estimated to be 5 - 10 pF. Hence the integration op-amp requires a higher gain-bandwidth product. Fig. 3.19 and Table 3.6 respectively show the schematic and parameters of the integration op-amp. A nulling resistor is put in series with the Miller capacitor to improve the frequency response, and a 30

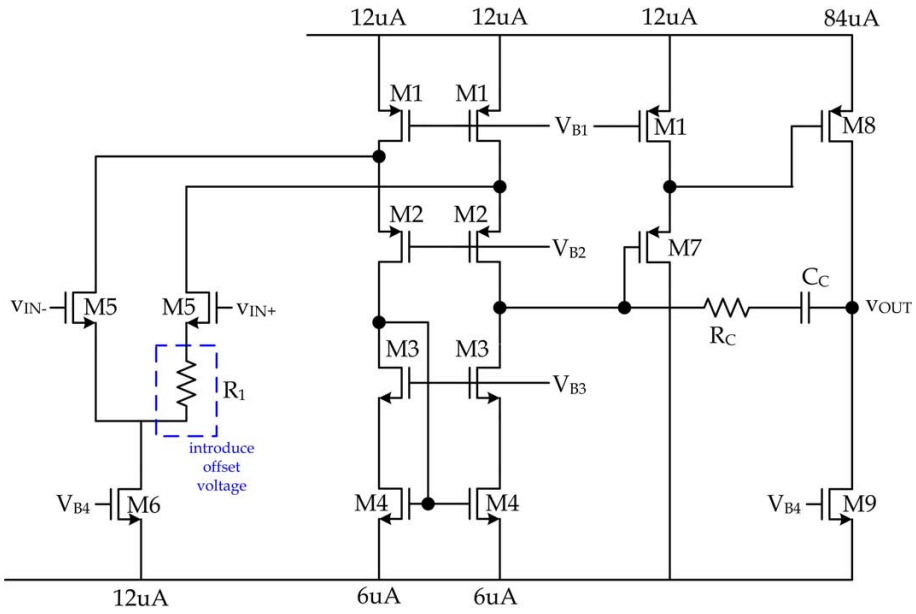

Figure 3.19: Schematic diagram of integration op-amp.

mV system offset voltage is introduced by resistor R_1. The frequency response of the op-amp is simulated using ($C_{LOAD} = 5\ pF$) and ($C_{LOAD} = 10\ pF$) and the results summarized in Table 3.7.

Transistor	M1	M2	M3	M4	M5
Sizing (um)	40/3.5	20/1	12/1.5	8/7	20/2
Transistor	M6	M7	M8	M9	
Sizing (um)	16/7	40/0.5	400/1	112/7	
Component	C_C	R_C	R_1		
Parameter	2 pF	500 Ω	7 $k\Omega$		

Table 3.6: Parameters of integration op-amp.

C_{LOAD}	5 pF	10 pF
Unit Gain Frequency (UGF)	4.739 MHz	4.618 MHz
Phase Margin	84.03^o	74.65^o
DC Gain	137 dB	137 dB

Table 3.7: Frequency response of integration op-amp.

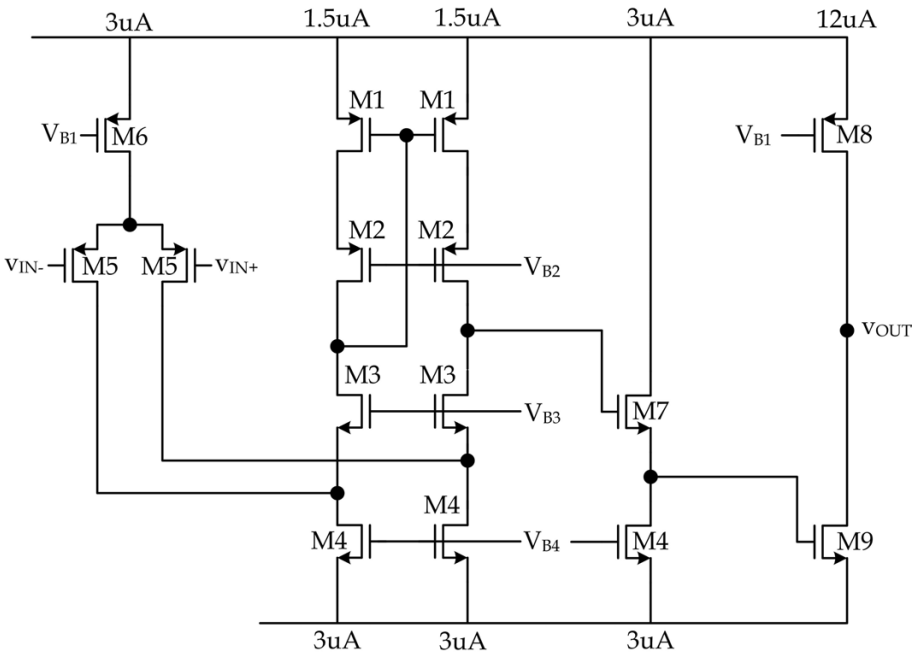

Figure 3.20: Schematic diagram of comparator.

Comparator

The comparator in our dual slope ADC has a input range 1 to 2 V (-1 to 0 V relative to A_{GND}). Hence, a PMOS input differential pair should be used. Fig. 3.20 and Table 3.8 shows the schematic and parameter of comparator respectively. The comparator employs a folded cascode first stage, a level shifter and a simple second stage.

The simulated DC gain (over 150 dB) is high enough to dominate the input voltage noise. As an output flip flop is used in the ADC to reduce capacitive load (C_{LOAD}) of the comparator, the worst case capacitive load is estimated to be 0.1

Transistor	M1	M2	M3	M4	M5
Sizing (um)	5/3.5	5/1	1.5/1.5	4/7	32/2
Transistor	M6	M7	M8	M9	
Sizing (um)	10/3.5	10/0.5	40/3.5	28/2	

Table 3.8: Parameters of comparator.

pF. Transient simulations are run to estimate the comparator propagation delay at 0.1 pF load and they are summarized in Table 3.9. The worst case delay (177 ns) is much shorter than one master clock period (1/204.8 kHz = 4.88 us), so the comparator is sufficiently fast for our application.

	Rise	Fall
input 50 % to output 50 % propagation delay (t_{PD})	177 ns	49.7 ns
output 10 % to 90% (90 % to 10 %) delay (t_P)	50.1 ns	2 ns

Table 3.9: Simulation results of comparator.

Integrating Capacitor

The off-chip integration capacitor plays an important role in the accuracy of our ADC. The capacitor leakage should be small so that charge stored during integration is preserved. This is easy to achieve using ceramic or polymer capacitors. However, the accuracy of the dual slope ADC is also affected by the dielectric absorption effect of the capacitor, which is often under estimated by designers.

Dielectric absorption is the process where electromagnetic energy stored in a capacitor is absorbed by dielectrics. We can model the dielectric absorption effect by adding additional resistors and capacitors in the capacitor as shown in Fig. 3.21 [28].

Although dielectric absorption is critical to our ADC accuracy, the information is usually not available in the specifications provided by the manufacturer. The

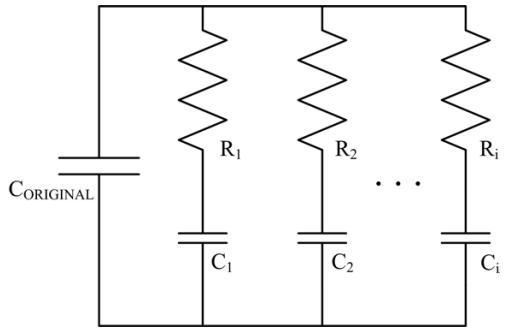

Figure 3.21: Modeling the dielectric absorption effect in a capacitor.

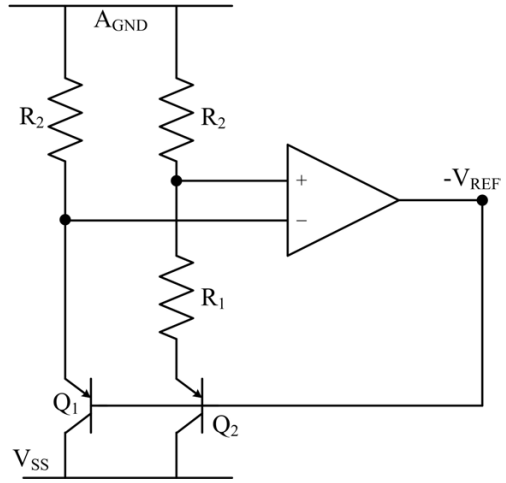

Figure 3.22: Simplified schematic diagram of negative voltage reference.

polypropylene capacitor used in our ADC is reported to have the lowest dielectric absorption [33].

Negative voltage reference

From Fig. 3.16 we found that a negative voltage reference (-1.21 V relative to analog ground A_{GND}) is needed in the ADC. The voltage reference should be stable when loaded with a 1 $M\Omega$ resistive load (R_{INT}). We have developed a negative voltage reference using a 2-stage op-amp, resistors and PNP transistors, the simplified schematic is shown in Fig. 3.22.

The simulated temperature dependence of the negative voltage reference under a 1 $M\Omega$ resistive load is shown in Fig. 3.23. The simulated temperature coefficient

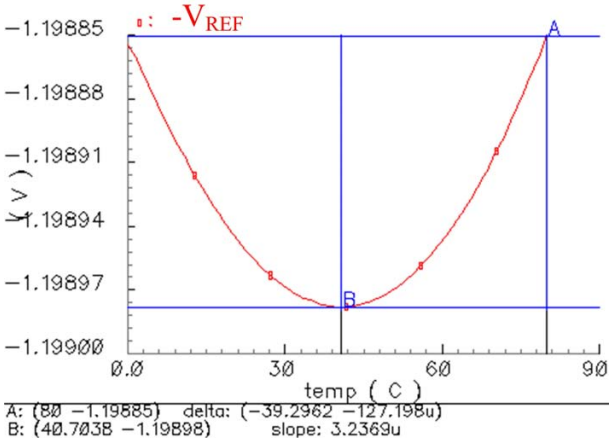

Figure 3.23: Simulated temperature dependence of negative voltage reference.

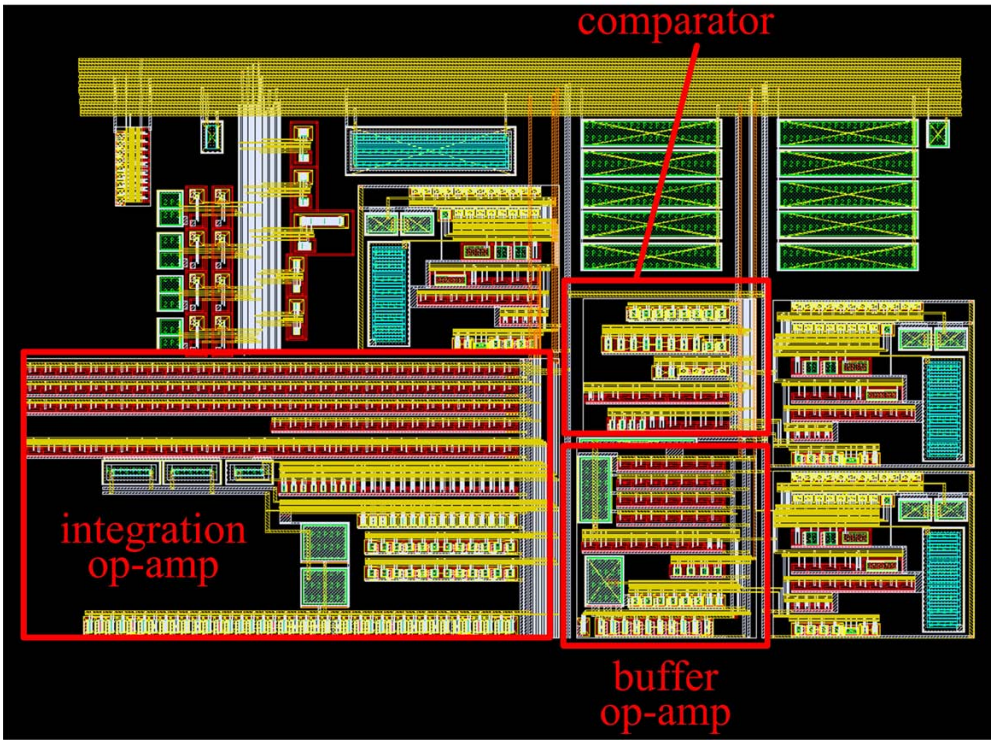

Figure 3.24: Layout of dual slope ADC.

is 1.3 $ppm/℃$ and estimated to be $\sim$ 50 $ppm/℃$ in the fabricated device due to mismatch. The negative voltage reference is not put on our prototype due to area constraints, and an off-chip voltage reference is used instead.

Layout out of ADC

The ADC layout is done carefully following the general matching rules in reference [17]. Fig. 3.24 shows the layout of ADC.

3.3.5 Power Consumption of CNT-CMOS IC

The simulated power consumption of the dual slope ADC and programmable current source are 116.9 uA and 34.71 uA respectively. The simulation conditions are temperature = 27 ℃ and $I_{OUT} = 0$ uA. The total power consumption is 755 uW.

3.3.6 Electrodes for CNT Sensor Formation

Geometrical constraints of electrodes in CMOS process

The resolution of top metal layer in any modern CMOS process surpasses the requirements for CNT sensor electrodes, which require 2 - 3 um separation. However, the passivation layer, used in all standard chips introduces other constraints. Fig. 3.25 shows a trivial construction of CNT electrodes in a CMOS process, it will not work because passivation layer etchant will attack the underlaying oxide layer through the opening on the top metal layer (metal is a etch stopper for passivation etchant) and the entire chip will be destroyed. For this reason, top metal openings are not allowed in a passivation opening in modern CMOS process design rules.

The problem can be solved by modifying the fabrication process so that the passivation layer is not used in the IC. As we are using multi projects on a single wafer process, we are not allowed to do so. Thus, we have to put the electrodes

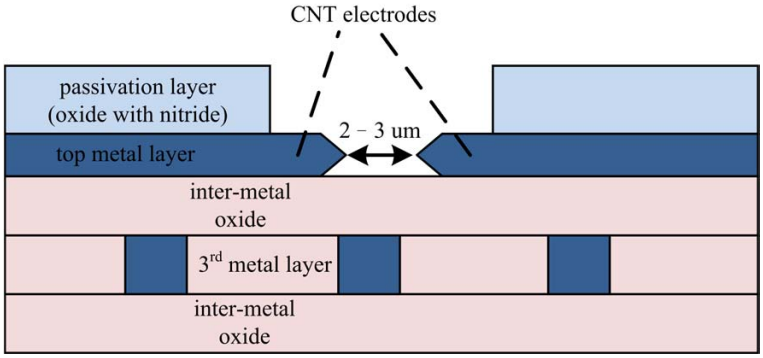

Figure 3.25: Unfeasible CNT electrodes configuration in CMOS process (cross-sectional view).

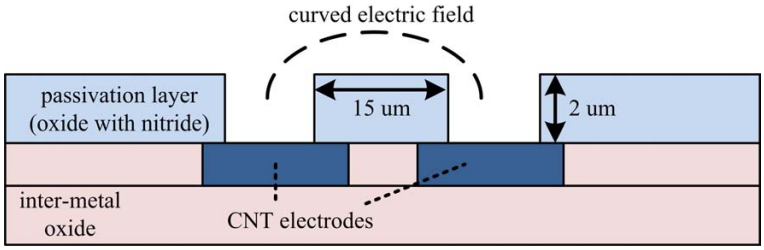

Figure 3.26: CNT electrodes in standard CMOS process with separate passivation openings (cross-sectional view).

in separated passivation openings, as illustrated in Fig. 3.26. This configuration introduces uncertainty to CNT formation because the CNTs and electric field have to bend around the passivation layer which is $\sim 2\ um$ in height and $15\ um$ in width. The layout of CNT electrodes in our prototype is shown in Fig. 3.27.

The AC voltage for DEP force CNT sensor formation is supplied to the CNT electrodes through two bare bonding pads, their electrostatic discharge (ESD) protection circuitry was omitted for two reasons. Firstly, CNT sensor are resistive and there is no evidence that they will be damaged by ESD. Secondly, $\sim 10\ V$ (peak-to-peak) AC voltage is applied to the bonding pads during CNT sensor formation. This will damage ESD protection circuits. Another solution is to use a high voltage process such as AMS® H35B4D3 process [8], however, this will lead to an increase in cost.

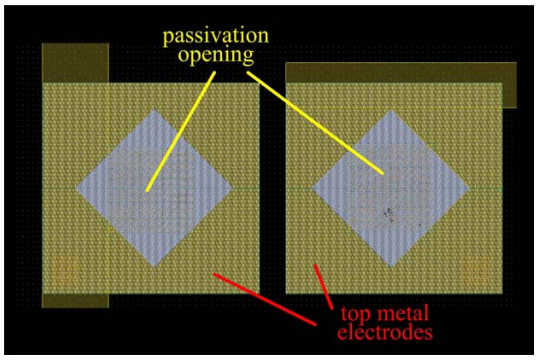

Figure 3.27: Layout of CNT electrodes.

Post-Fabrication Plating Process for Electrodes

In a standard CMOS process, aluminium is used for all metal layers (copper is only used in high-end digital processes). Unfortunately, aluminium is easily oxidizes in air, and form an insulator on the contacts between electrodes. Hence the CNT sensor cannot be formed using aluminium electrodes. We cannot solve the problem by removing the aluminium oxide layer using solely mechanical or chemical methods because the oxide layer will quickly reform. A post-fabrication plating process is required to remove the oxide.

A series of chemical plating steps is used to attach gold on the electrodes. Unlike an electroplating process, high voltage is not necessary for chemical plating and hence the circuits are preserved in the process. Before we start the process, the chip is immersed in 50% nitric acid (NHO_3, room temperature) for 15 seconds to remove the aluminium oxide. The chip is then washed in water and immersed in a "zincate" solution for 20 seconds (at room temperature). A thin layer of the aluminium will be replaced by zinc and the reaction stops once the whole electrode is covered. The chemical reaction can be represented by:

$$2Al + 3Zn^{2+} \longrightarrow 2Al^{3+} + 3Zn \downarrow \tag{3.16}$$

A nickel metal layer is required before the gold plating process. We immerse the chip in a chemical solution at 85 ℃ for 5 minutes. A nickel metal layer is

plated on the zinc layer and the reaction is described by:

$$\begin{cases} [H_2PO_2]^- + H_2O \overset{catalyst}{\longrightarrow} H^+ + [HPO_3]^{2-} + 2H \\ Ni^{2+} + 2H \longrightarrow Ni \downarrow + 2H^+ \end{cases} \tag{3.17}$$

Finally, the chip is immersed in a gold plating solution at 75 ℃ for 3 minutes. Gold particles replace the zinc layer and a gold layer is left on the aluminum electrodes. The chemical reaction in the process is represented by:

$$Ni + 2Au^+ \overset{catalyst}{\longrightarrow} Ni^{2+} + 2Au \downarrow \tag{3.18}$$

3.3.7 Electrostatic Discharge Protection and Layout of Prototype

Electrostatic Discharge Protection and I/O Pads

ESD Protection is necessary for each I/O (input / output) pin in integrated circuit. An ESD protection circuit is usually included in the bonding pad of an I/O pin. It provides additional current paths between the pad and supply rails and is activated in an ESD event [46]. Each I/O pad is connected to one positive supply rail and one negative supply rail through its ESD circuits, and each supply rail is connected to its complementary supply rails through its ESD circuit.

The I/O pins in the prototype IC are divided into analog and digital domains so that digital noise is not coupled into the analog circuits, Table 3.10 shows the I/O pins belonging to the analog domain and their ESD circuits are connected to the analog positive supply (A_{VDD}) and analog negative supply (A_{VSS}). Table 3.11 shows I/O pins for the digital domain and their ESD circuits are connected to the digital supply (V_{DD} and V_{SS}). Table 3.12 shows all supply I/O pins and the ESD connections between them.

Pin	Description
C_1	control for $\times 1$ current mirror
C_2	control for $\times 2$ current mirror
C_4	control for $\times 4$ current mirror
C_8	control for $\times 8$ current mirror
C_{16}	control for $\times 16$ current mirror
C_{32}	control for $\times 32$ current mirror
C_{64}	control for $\times 64$ current mirror
C_{128}	control for $\times 128$ current mirror
I_{OUT}	output of programmable current source
V_{REF}	input for -1.21 V voltage reference
v_{IN}	input for CNT sensor
C_{INT+}	+ve terminal of integration capacitor
C_{INT-}	-ve terminal of integration capacitor
T_2	test point 2
T_5	test point 5

Table 3.10: Analog I/O pins.

Pin	Description
v_{OUT}	output of comparator
S_1	control for switch S_1 and $\overline{S_1}$
S_2	control for switch S_2
S_3	control for switch S_3
S_4	control for switch S_4
CLK	clock input for output flip-flop

Table 3.11: Digital I/O pins.

Pin	Description	Pad Type	Voltage	ESD connected to
A_{VDD}	analog +ve supply	VDD Pad	5 V	A_{VSS}
A_{VSS}	analog -ve supply	GND Pad	0 V	A_{VDD}
A_{GND}	analog ground	VDD Pad	2 V	A_{VDD}
V_{DD}	digital +ve supply	VDD Pad	5 V	V_{SS}
V_{SS}	digital -ve supply	GND Pad	0 V	V_{DD}

Table 3.12: Supply pins

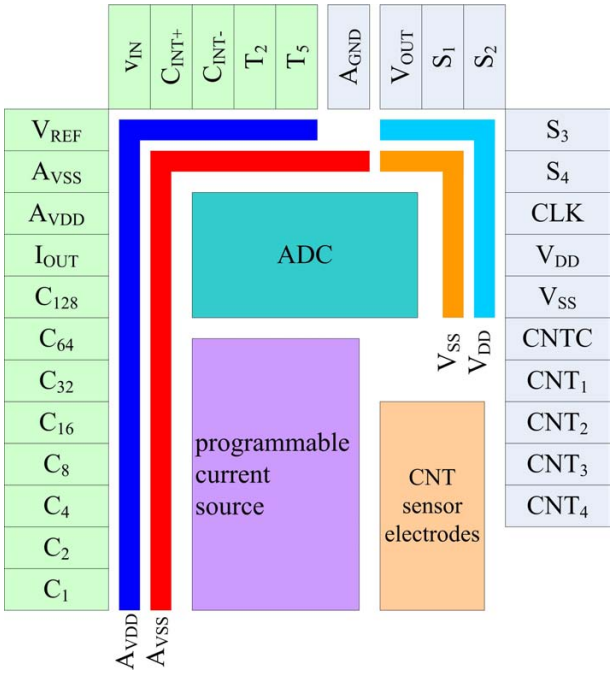

Figure 3.28: Floor plan of our prototype.

Layout of Prototype

The floor plan of the IC is shown in Fig. 3.28. Two sets of supply rails (V_{DD} and V_{SS}, A_{VDD} and A_{VSS}) are connected to the ESD protection circuits of the I/O pins following table 3.10 - 3.12. They are also connected to the the ADC and programmable current source. The four CNT electrode pairs share one common ground I/O pin ($CNTC$) and have different positive terminals ($CNT_{[1..4]}$). Fig. 3.24 shows the entire layout of our IC prototype.

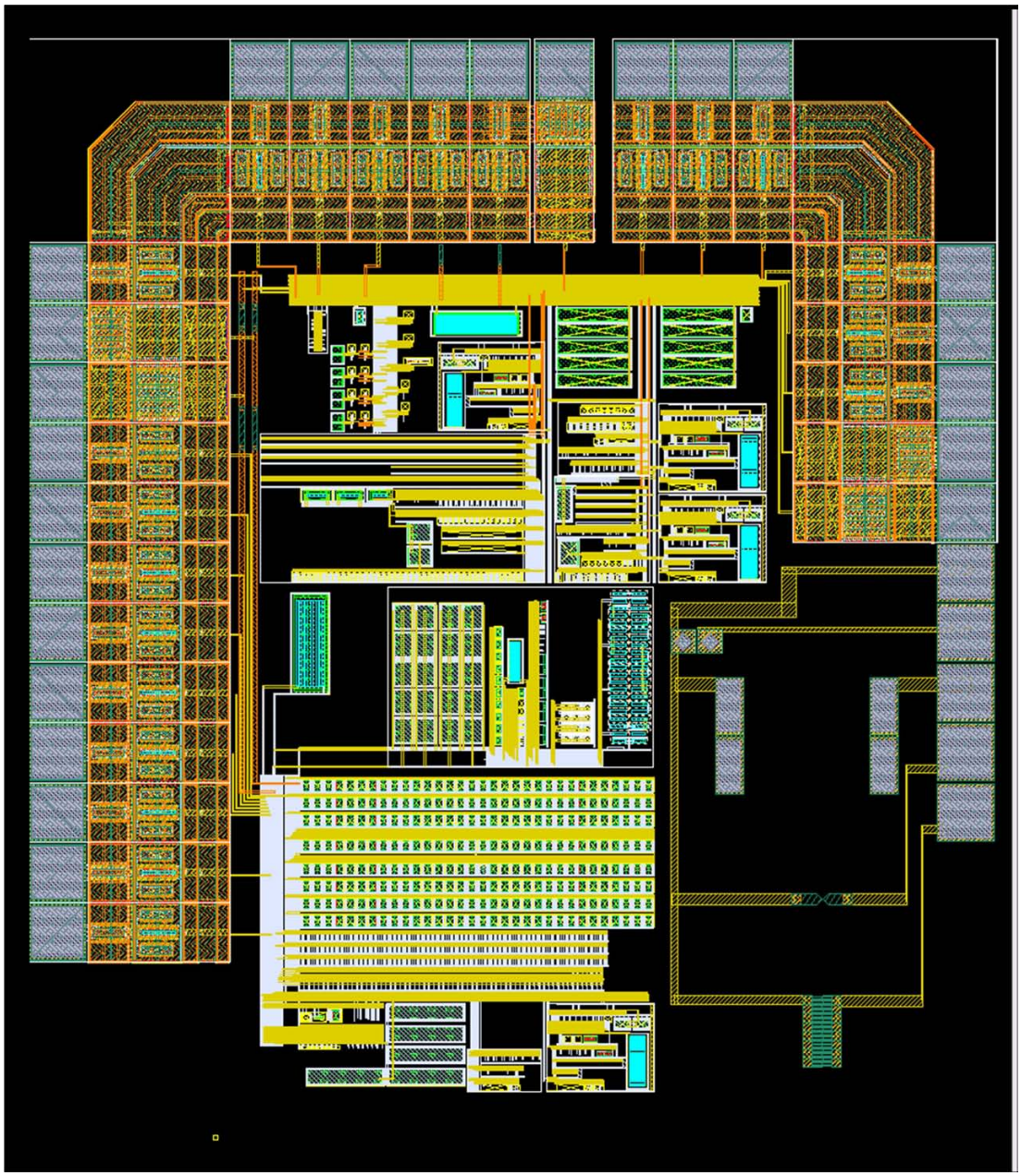

Figure 3.29: Layout of IC prototype.

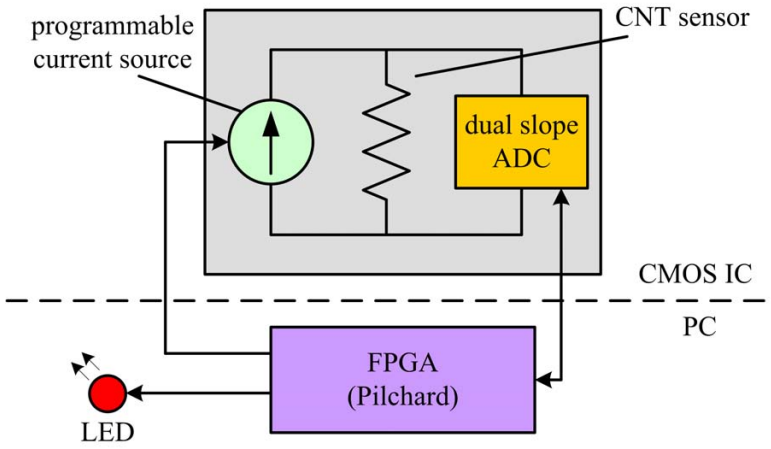

Figure 3.30: Architecture of alcohol tester for driver.

3.4 Alcohol Tester

In a traditional alcohol tester, high power consumption is required to generate heat to remove attached alcohol molecules on the sensor. CNT alcohol sensors have the advantage of low power consumption because it is easily self-heated and is hence a good application to show the potential of CNT-CMOS integrated sensor [37].

We propose an alcohol tester for driver using our CNT-CMOS integrated sensor. The architecture is shown in Fig. 3.30. The programmable current source, ADC and light emitting diode (LED) are controlled by the FPGA. To simplify the development, a Pilchard FPGA development board [24] is used to collect data from the FPGA through a personal computer (PC).

3.4.1 Operation of Alcohol Tester

The operation of our alcohol tester can be divided into 4 stages, they are the manufacturer calibration stage, the self-calibration stage, the alcohol testing stage and the annealing stage.

The manufacturer calibration stage is executed every time a new CNT-CMOS integrated sensor is connected to the system. In this stage, the following sensor

dependent parameters are input to the system:

- $I_{MEASURE}$, the current used for alcohol detection.
- I_{ANNEAL}, the current used to remove attached alcohol vapor.
- $R_{THRESHOLD}$, a threshold value (measured in relative CNT resistance change) to indicate illegal alcohol levels in the driver.

The tester will enter the self-calibration stage every time it is turned on. A constant current equal to $I_{MEASURE}$ will bias the CNT sensor, and the ADC will convert the voltage across the CNT 10 times. The CNT initial resistance ($R_{INITIAL}$) is calculated using the average value of the ten measurements. Self-calibration is necessary because it reduces problems associated with different environmental temperatures and long term sensor drift.

When the tester is turned into an alcohol testing stage by the user, the ADC will continuously sample the voltage across the CNT sensor with at a sampling rate of 5 Hz for 10 seconds. The driver should blow air onto the sensor during this period. The CNT resistance (R_{CNT}) are calculated from the sampled voltage. The resistance change (measured in %) of CNT resistance is displayed on the computer. If any calculated resistance change exceeds ($R_{INITIAL}$) by ($R_{THRESHOLD}$) percent, a LED will be turned on to indicate a dangerous alcohol level.

The tester will then be put into the annealing stage automatically. In the annealing stage, the CNT sensor is biased by a much larger current (I_{ANNEAL}) for 30 seconds and the temperature of the sensor will rise. Attached vapor molecules will be removed and resistance of the CNT will return to the initial value.

3.5 Summary

In this chapter, we introduced the novel idea of CNT-CMOS integration and defined the goal of first prototype IC. The design and analysis of 3 major components in our IC, the programmable current source, ADC and electrodes were

given. We also proposed a chemical plating process to solve the problem of electrodes oxidation. Finally, we proposed an alcohol tester for driver to demonstrate a CNT-CMOS integrated sensor system.

Chapter 4

Results

4.1 Introduction

In this chapter, the testing results from the fabricated IC are presented. We tested the performance of the current source and the ADC, and we also formed a CNT sensor on our IC prototype using a chemical process. Although some parameters of the current source and ADC deviated from their design specifications, we show the feasibility of CNT-CMOS integration through our IC. The CNT-CMOS IC can be improved in future prototypes or products based on the results obtained. Finally, we test functionalities of the alcohol tester by carbon film resistor.

4.2 Chip Package and Photography

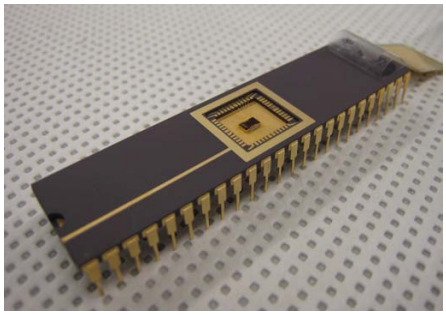

Figure 4.1: Prototype IC package in DIP48 package.

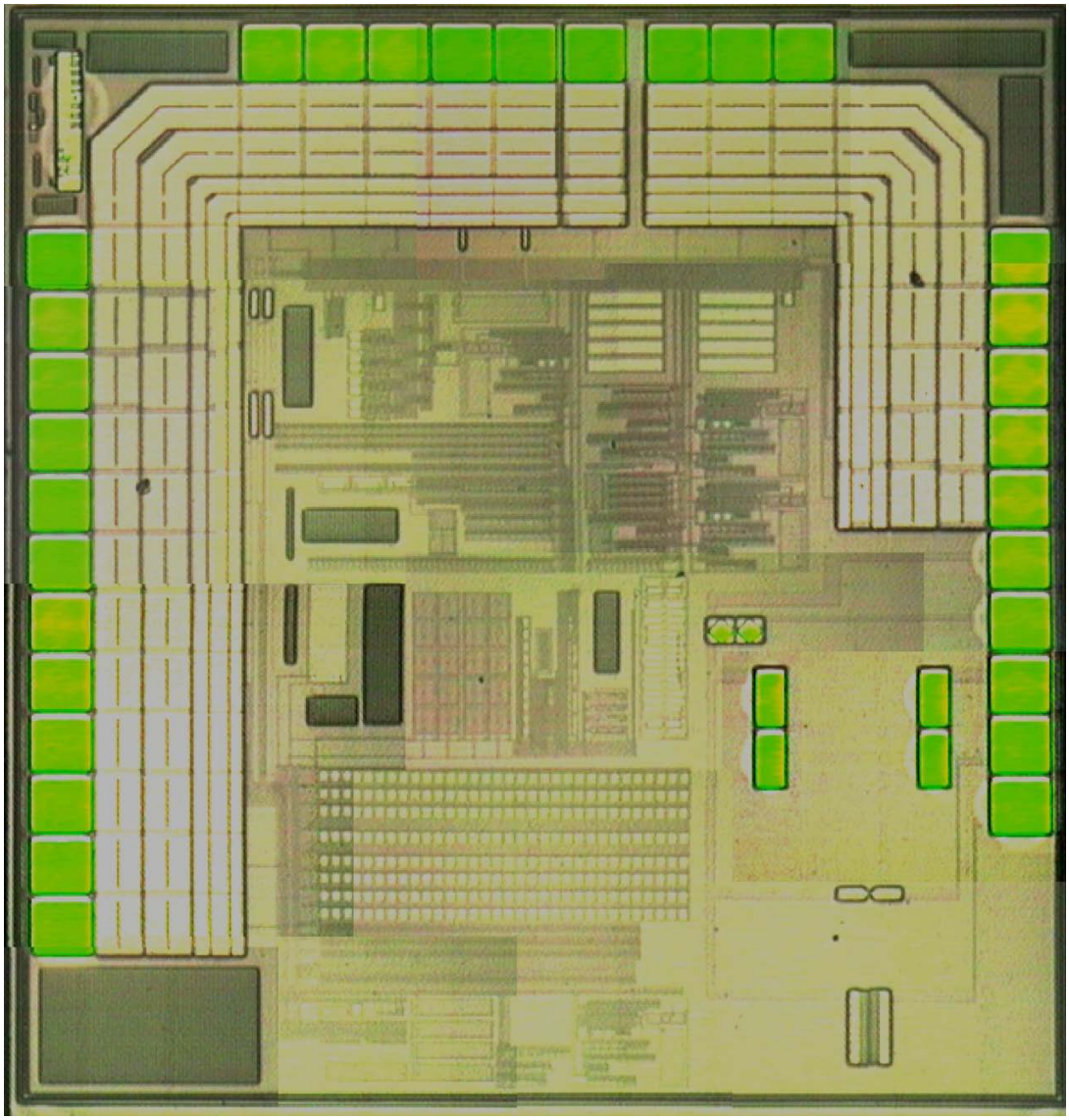

Figure 4.2: Photomicrograph of IC prototype.

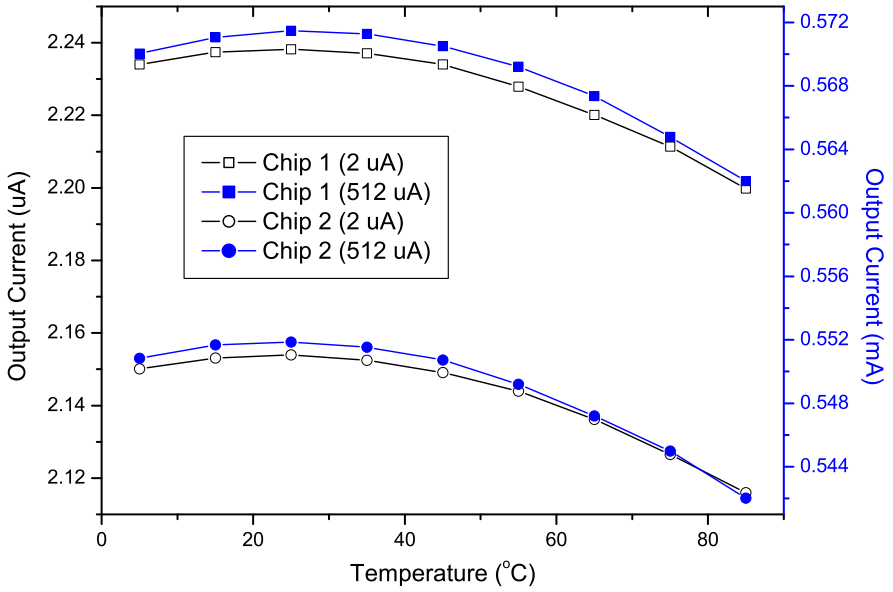

Figure 4.3: Measured temperature dependence of fabricated programmable current source.

There are 26 I/O pins in our IC prototype, hence a 48 pins Dual-In-Line-Package (DIP) is chosen. Reduced packages such as the Small Outline Integrated Circuit (SOIC) [20] can be used in production to reduce size of the chip. Fig. 4.1 show our packaged IC. The photomicrograph of the IC is shown in Fig. 4.2.

4.3 Results from Programmable Current Source

4.3.1 Temperature Coefficient

Two fabricated prototypes are put into a controlled temperature and humidity chamber [3]. The relative humidity is set to 35%, the temperature of the chamber swept from 5 ℃ to 85 ℃, and the output voltage (V_{OUT}) set to 1 V. The measured temperature dependence of the programmable current source using a sourcemeter is shown in Fig. 4.3.

The two prototypes show significantly different reference currents ($\sim 2.24\ uA$

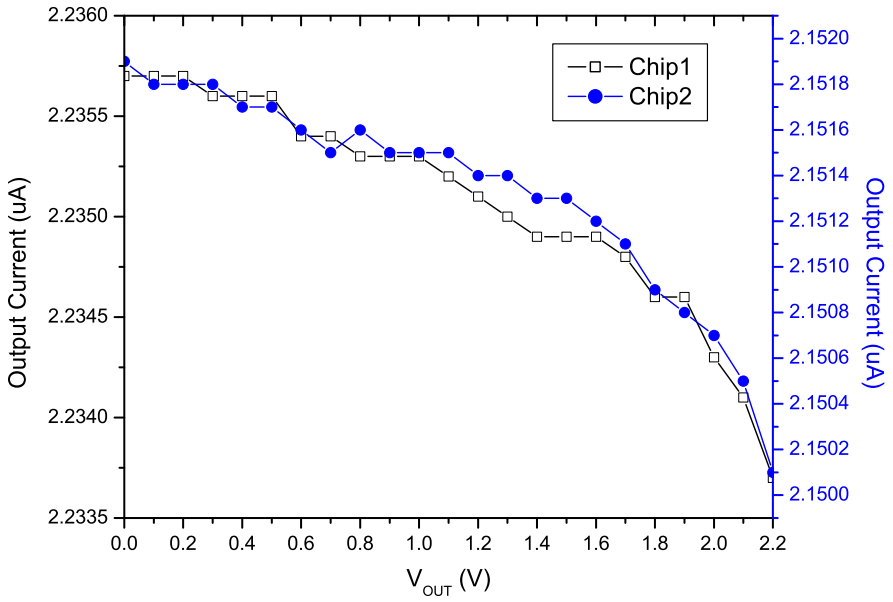

Figure 4.4: Measured voltage dependance of programmable current source.

for chip 1 and $\sim 2.15\ uA$ for chip 2) due to process variation. All the 4 measured curves show a $\sim 240\ ppm/$℃ temperature coefficient compared with $\sim 80\ ppm/$℃ temperature coefficient in our simulations.

The unexpectedly high temperature coefficient of the current source may be explained by two factors. I) Mismatch in the modified bandgap voltage reference making its temperature coefficient differ from the designed value, II) Error in the high-resistance poly temperature coefficient model used in the simulations. Both errors affect the balance between the temperature coefficient of the voltage reference and high-resistance poly in the V to I converter, causing an increase in the resulting temperature coefficient of the current source.

4.3.2 Output Resistance

We also measure the output resistance of the programmable current source using the sourcemeter. The measurements are conducted at 20 ℃ and 40% relative

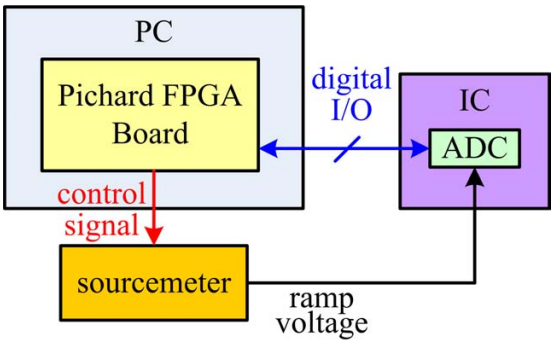

Figure 4.5: Architecture of ADC testing system.

humidity. The output current (I_{OUT}) is set to 2.1 uA while the output voltage (V_{OUT}) is swept from 0 V to 2.2 V. The results are shown in Fig. 4.4. The measured output resistance is 120.9 $M\Omega$ (chip 1) and 137.5 $M\Omega$ (chip 2), which is high enough for all CNT sensors.

4.4 Results from Dual Slope ADC

The dual slope ADC is tested using a Pilchard FPGA board [24] and a sourcemeter. Fig. 4.5 shows the architecture of our testing system. The digital control of the ADC is implemented using Pilchard. The computer controls the sourcemeter to output a ramp voltage from 0 V to 2.1 V (in 50 uV step) to the ADC. The ADC code words at different voltages are recorded by the computer for further processing. The sourcemeter has a 50 uV programming resolution and 50 uV output noise reported by the manufacturer [21]. However, the actual output noise maybe much higher due to environmental noise. The schematic diagram of testing system is shown in Appendix A. The pseudo code for ramp voltage generation and data recording is shown in Algorithm 1. A photograph of the whole setup is shown in Fig. 4.6.

The accuracy of an ADC can be classified into DC and dynamic specifications [44]. As the sampling rate of our ADC is low and we are only interested in DC measurement, only the ADC DC specifications are tested. These can be

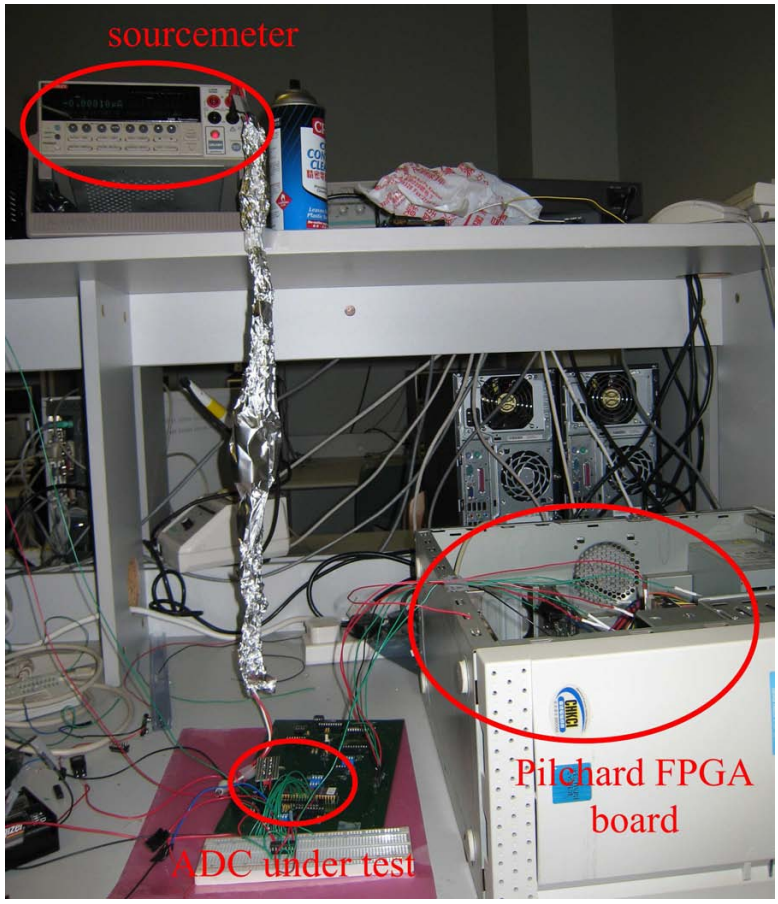

Figure 4.6: ADC testing system.

Algorithm 1 ADC Testing

BEGIN
$V_{OUT} \leftarrow 0\ V$
while $V_{OUT} \leq 2.1\ V$ **do**
  set sourcemeter output to V_{OUT}
  wait 100 ms
  reset ADC
  start ADC conversion
  wait 50 ms
  read ADC output code word (ADC_{OUT})
  store V_{OUT} and ADC_{OUT} to file
  $V_{OUT} = V_{OUT} + 50\ \mu V$
end while

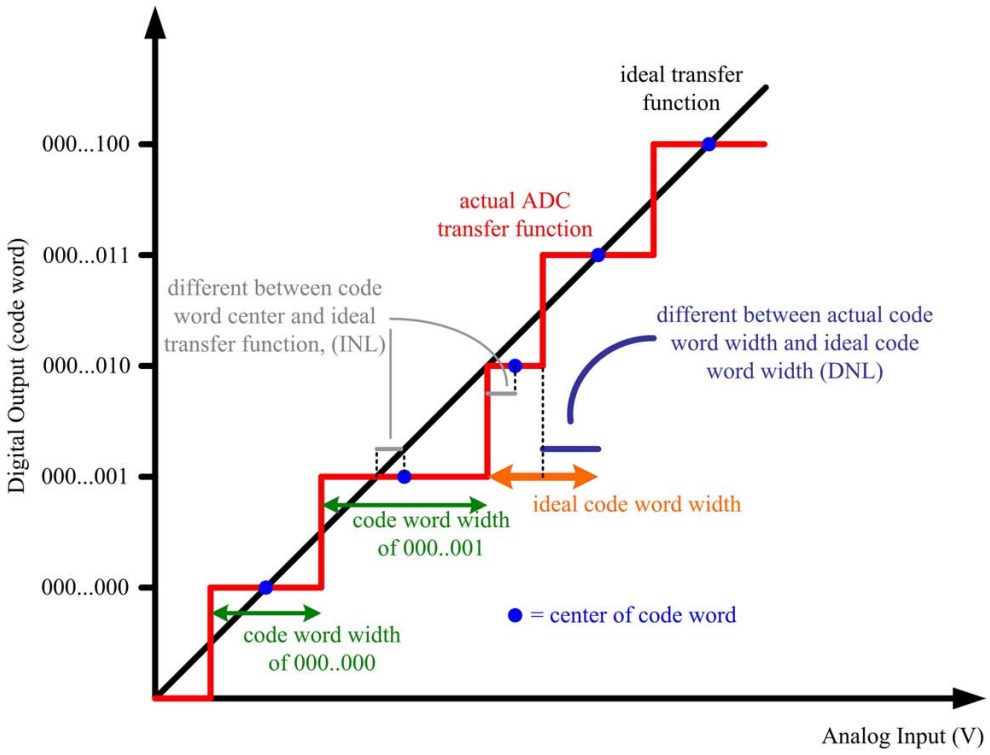

Figure 4.7: Illustration of DNL and INL of an ADC.

characterized by the differential nonlinearity (DNL) and the integral nonlinearity (INL) [44]. DNL is the different between actual code word width and ideal code word width. INL is the deviation of the ADC transfer function from the ideal transfer function, Fig. 4.7 illustrate the definition of DNL and INL. Both of them are normalized to one least significant bit (LSB) [44].

Although our ADC is designed to measure input voltage up to 2.42 V, the sourcemeter can only provide sufficiently small programming resolution in the range of 0 - 2.1 V, hence we only tested the ADC in this range. In our testing, the transition boundary (measured in V) of every code word is calculated by the following equations:

$$B_L[i] = min(v|_{code\_word=i}) - \frac{50uV}{2} \tag{4.1}$$

$$B_U[i] = max(v|_{code\_word=i}) + \frac{50uV}{2} \tag{4.2}$$

where

$B_L[i]$ and $B_U[i]$ are the lower and upper boundary of code word i.

$min(v|_{code\_word=i})$ is the minimum v_{in} converted to code word i.

$max(v|_{code\_word=i})$ is the maximum v_{in} converted to code word i.

As the programming resolution of the sourcemeter is 50 uV, there exist +/- 25 uV uncertainty at the output of sourcemeter, hence 25 uV is added or subtracted in the equations to reflect the uncertainty.
The width of each code word i ($code_W[i]$) is defined as:

$$code_W[i] = B_U[i] - B_L[i] \tag{4.3}$$

The center of each code word i ($code_C[i]$) is defined as:

$$code_C[i] = \frac{B_U[i] + B_L[i]}{2} \tag{4.4}$$

In our testing, **end points DNL and INL** defined in reference [44] is adopted. The ideal transfer function illustrated in Fig. 4.7 is constructed by joining the measured offset point ($code_C[0]$) and measured full scale point ($code_C[full]$, $full$ is the code word of $v_{IN} = 2.1\ V$).

The ideal code word width ($code_W|_{IDEAL}$) is calculated from Eq. 4.5 and the DNL of each code word can be calculated using Eq. 4.6:

$$code_W|_{IDEAL} = \frac{code_C[full] - code_C[0]}{full} \tag{4.5}$$

$$DNL[i] = code_W[i] - code_W|_{IDEAL} \tag{4.6}$$

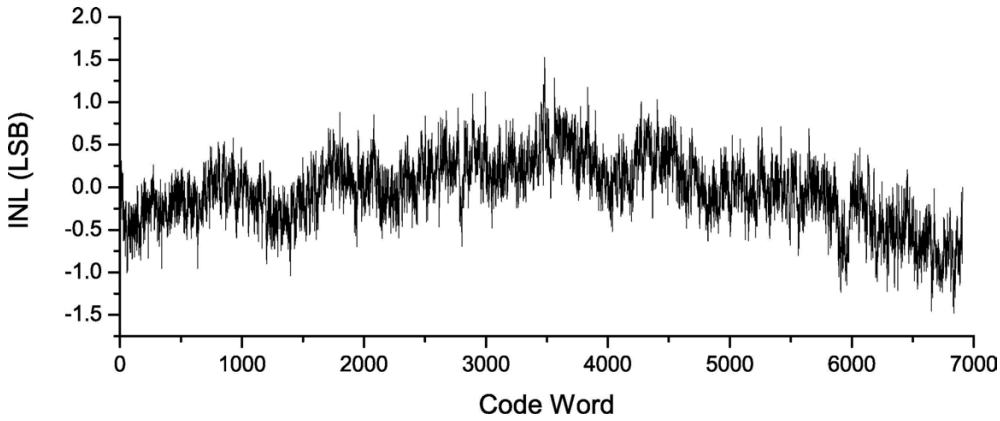

Figure 4.8: Measured INL of the dual slope ADC.

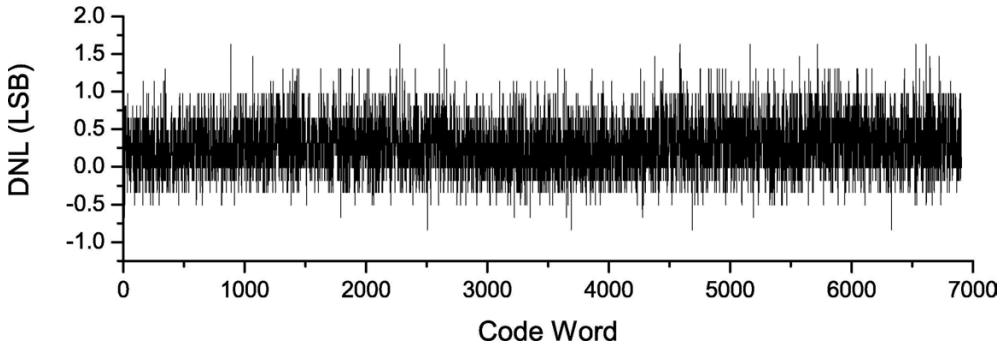

Figure 4.9: Measured DNL of the dual slope ADC.

where

$DNL[i]$ is the DNL of code word i.

The ideal code word center of i ($code_C|_{IDEAL}[i]$) is calculated from Eq. 4.7 and the INL of each code word can be calculated using Eq. 4.8:

$$code_C|_{IDEAL}[i] = code_C[0] + i \times code_W|_{IDEAL} \tag{4.7}$$

$$INL[i] = code_C[i] - code_C|_{IDEAL}[i] \tag{4.8}$$

where

$INL[i]$ is the INL of code word i.

From our testing, the measured DNL of our ADC is between -0.84 LSB and

1.63 LSB as can be seen in Fig. 4.9. The measured INL is -1.48 LSB to 1.52 LSB as shown in Fig. 4.8.

The effective number of bits (ENOB) can be calculated from the INL using the following equation [44]:

$$ENOB = B_{DESIGNED} - \frac{log(1 + 3 \times |INL|^2)}{2log2} \tag{4.9}$$

where

$B_{DESIGNED}$ is the designed number of bits

$|INL|$ is the maximum absolute INL

From the equation, we found that the ENOB of the ADC is 11.5 bit. Possible reasons of accuracy reduction include device mismatch and other parasitic effects that are not included in our ADC simulation setup.

4.5 Power consumption of the Integrated Circuit

The power consumption of the IC is measured at temperature = 25 ℃ and I_{OUT} = 0 uA and seen to be 1.22 mW. The difference between the simulated result (755 uW) and measured result maybe due to leakage, device mismatch and process variation. However, both results show a low power consumption sensor systme. A power down mode can be added to reduce standby power.

4.6 CNT Sensor Formation

The chemical gold plating process described in Section 3.3.6 is a necessary step which must be applied prior to CNT sensor formation using the DEP process. Unfortunately, the process may destroy the bonding wires in a packaged IC so

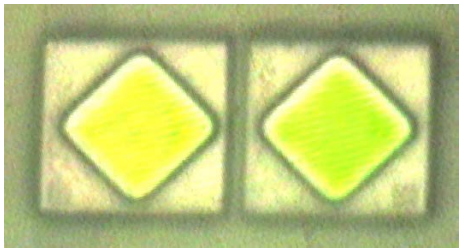

Figure 4.10: Unmodified CNT sensor electrodes in IC prototype.

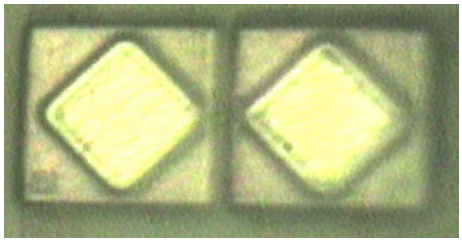

Figure 4.11: A CNT electrode pair after chemical gold plating.

bare dies are used.

Fig. 4.10 shows an unmodified CNT sensor electrode pair, the electrodes are covered by an aluminium oxide layer and it does not conduct electricity. An electrode pair after the plating processes is shown in Fig. 4.11. Parts of the electrodes become dark in color due to uneven metal plating.

The plating process deposits two metal layers (zinc and gold) on top of the aluminium bonding pads. We use probes to make electric connections to the bare die. A bare die connected by micro probes is shown in Fig. 4.12. Note that the conductivity between electrodes is zero before the DEP process.

The plating process should be well controlled to prevent over-deposition of gold. Fig. 4.13 shows electrodes which are over-plated and shorted together.

The DEP process for CNT formation described in section 2.4.1 is used for CNT sensor formation in the bare die. MWNTs from the Sun Nanotech Company Ltd., buffered in ethanol are used. An AC voltage voltage (1 MHz, 8 V_{pp}) is applied to the electrodes through the micro probe and a $\sim 50\ k\Omega$ (Fig. 4.14) CNT sensor is successfully formed (Fig. 4.15).

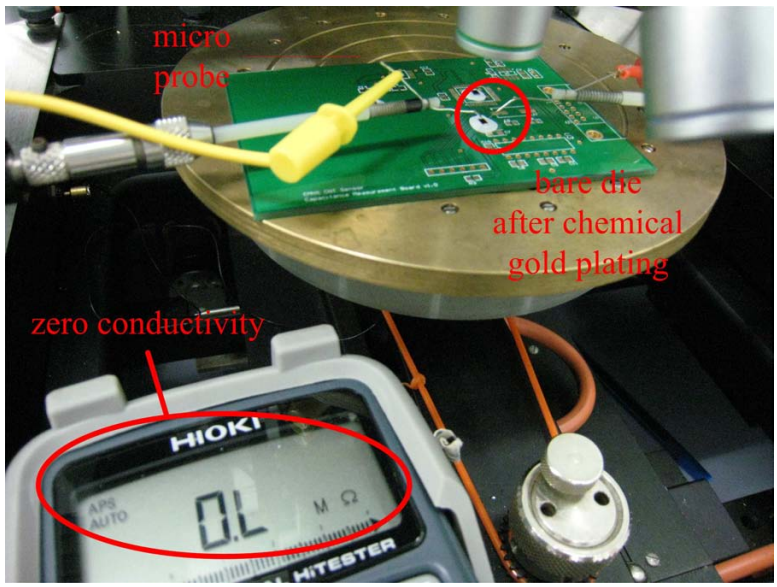

Figure 4.12: A bare die connected by micro probe.

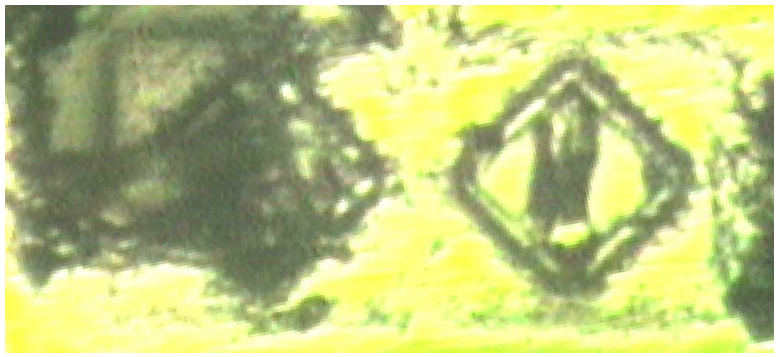

Figure 4.13: Electrodes connected by gold after gold plating process.

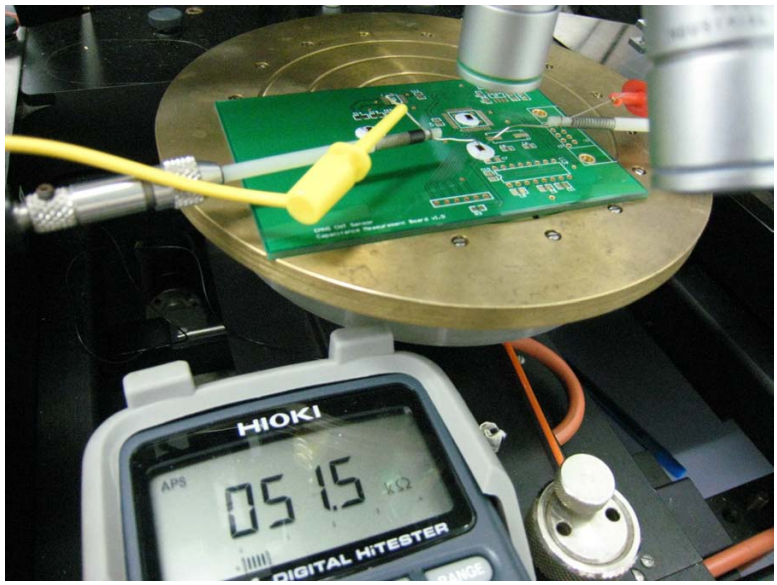

Figure 4.14: 50k resistance measured between electrodes.

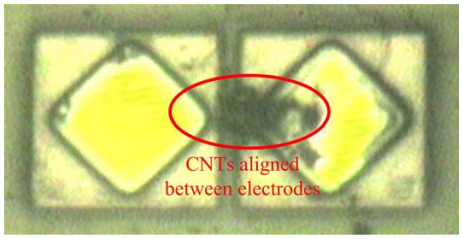

Figure 4.15: A CNT sensor on the electrodes of our prototype.

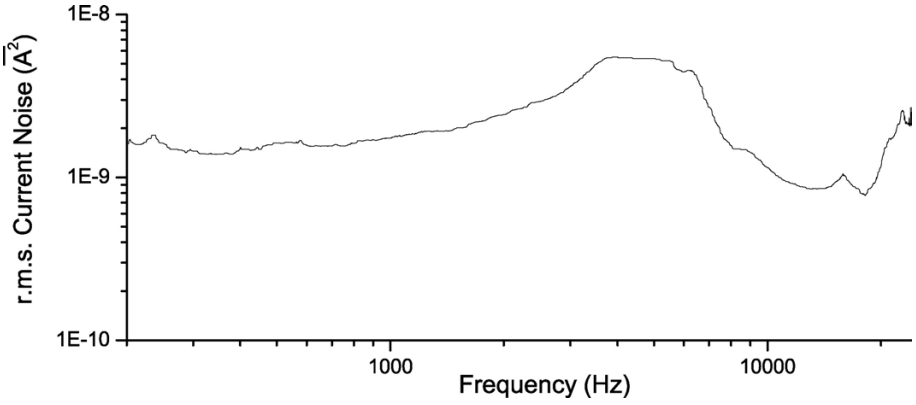

Figure 4.16: Current noise of a 40 $k\Omega$ metal film resistor on probe station.

4.6.1 Noise Measurement of CNT-CMOS Integrated Sensor

We attempted to characterize sensor noise on the CNT-CMOS using the experimental setup described in Section 2.6.2. The entire setup is not enclosed in aluminium box and hence no shielding was used. Fig. 4.16 shows the measured current noise of a 40 $k\Omega$ metal film resistor on the probe station. We found that the noise is $\sim$ 3 order of magnitudes higher than measured with shielding (Section 2.6.2). Hence, we conclude that we cannot measure noise of the CNT sensor using micro probes.

The resistance of the CNT sensor on our CNT-CMOS prototype is sampled using a sourcemeter 100 times with a sampling frequency of 1.43 Hz. The SNR of the sensor is calculated using Eq. 2.4 - 2.8 and found to be 54.6 dB. This is $\sim$ 10 - 20 dB lower than the CNT sensor we measured in Section 2.9.

4.7 Alcohol Tester Results

The alcohol tester proposed in Section 3.4 determines if the alcohol level of a driver exceeds a certain level by measuring the relative resistance change of CNT sensor. In this section, the ability of relative resistance measurement is demonstrated.

4.7.1 Carbon Resistor

Two carbon film resistors are used to model the change in resistance that a CNT sensor experiences when subjected to alcohol vapor. A 30 $k\Omega$ emulates the initial CNT sensor resistance and a 33 $k\Omega$ emulates the CNT in the presence of alcohol. The resistance of the two resistors are measured by the alcohol tester by setting $I_{OUT} = 10\ uA$, and reference measurements (with accuracy of $\sim 0.07\%$) are made using the sourcemeter. Table 4.1 summarizes results of the resistance measurement.

	30 $k\Omega$ resistor	33 $k\Omega$ resistor
sourcemeter measurement	30.387 $k\Omega$	32.92 $k\Omega$
difference in %	/	**8.336**
alcohol tester measurement (code word)	1117	1210
resistance	35.724 $k\Omega$	38.699 $k\Omega$
difference in %	/	**8.326**

Table 4.1: Resistance measurement results of alcohol tester and sourcemeter.

From Table 4.1, we found large errors in the absolute resistance measured with the alcohol tester. The errors can be explained by process variation affecting the 10 uA current source (i.e. actual $I_{OUT} \neq 10\ uA$) and offset voltage of the buffer op-amp in Fig. 3.16 (as seen in Eq. 3.13). However, the relative errors in resistance are 0.01%. We conclude that the alcohol tester is capable of measure relative resistance with sufficient accuracy for CNT sensor applicatons.

4.8 Summary

In this chapter, we presented the testing results from fabricated CNT-CMOS prototype chips. We found the current source has an output resistance of over 100 $M\Omega$ at 2 uA output current and the temperature coefficient of the current source was $\sim 240\ pm/$°C. The dual slope ADC was also tested and has an ENOB

not less than 11.5 bits. We proved the feasibility of the chemical gold plating process and formed CNT sensors on the bare dies of the prototype. Finally, we showed functionality of the alcohol tester by emulating CNT sensor resistance using carbon film resistors. We were not able to measure the CNT sensor noise spectrum due to difficulties associated with making resistance measurements on a probe station. We showed that this was also the case for a standard metal film resistor.

Chapter 5

Conclusion

The main objective of this work was determining the feasibility of CNT-CMOS integrated sensor. Several subproblems and original contributions were made to address different issues.

Noise in CNT sensors

Noise in traditional resistive sensors are well predicted by the thermal noise theory. $1/f$ noise of different magnitude are reported in carbon nanotube and carbon resistor in previous literatures. Frequency and bias current dependent noise which is one to two order of magnitude higher than traditional resistive sensor is observed in our CNT noise measurement. This work is the first reported noise measurement in CNT resistors fabricated by DEP process. The results explain the low SNR of DC measurement of CNT sensor reported by others and suggest that a high frequency CNT measuring technique may perform better.

CNT-CMOS Prototype IC

We developed a CNT-CMOS prototype IC, the prototype include a programmable current source, a dual slope ADC and CNT electrodes. The programmability of the current source allows us to measure the CNT sensor in self-heating or non-self-heating regions and the ADC provide reasonable accuracy for the CNT measurement.

The detailed design and analysis of our prototype is presented. Although some parameters of the fabricated device differ from the ideal values, we sucessful demonstrate the feasibility of CNT-CMOS integration.

Aluminium Oxidation of CNT Electrodes

Oxidation of aluminium electrodes is an unexpected problem we encounter in CNT-CMOS integration. We solved the problem by using a chemical gold plating process. This is an unreported problem and one of the key difficulties to integrate CNT sensor on commercial CMOS process.

Application of CNT-CMOS IC

To demonstrate the potential of the CNT-CMOS integrated sensor, an alcohol tester for driver is developed. We showed our CNT-CMOS IC is capable for the application. We can measure the CNT resistance using small output current from the current source and the ADC, the attached alcohol can be removed using large annealing current. We also showed that CNT sensor can be fabricated on the top of our IC after a chemical gold plating process. Although the size of the tester is not optimized due to the large digital control, it can be easily replaced by a on-chip one. We can also use a reduced package for the IC so that an CNT-CMOS integrated system with few mm^2 area is feasible.

5.1 Future Work

5.1.1 Detailed CNT Noise Characterization

Although we found frequency and bias current dependant noise in CNT sensor, the noise is also sensor dependant and we cannot find a mechanism for the noise characteristics. We suggest that detailed CNT noise characterization and modeling be studied.

5.1.2 High Frequency CNT Measuring Technique

Our findings of frequency dependent noise in CNT sensor suggest that we should measure the CNT resistance at higher frequencies. However, such measurements require an higher sampling rate ADC (10 - 20 kHz), some filtering circuitries and a more complex digital control. A delta sigma ADC is a good choice because it can provide sufficient resolution at the sampling rate. We may obtain better accuracy using the high frequency measurement.

5.1.3 Higher Degree of CMOS Integration

The size of CNT sensor system may be further reduced by higher degree of CMOS integration. The off-chip integration capacitor may be avoided by using different ADC architecture such as delta sigma ADC, the off-chip digital control can be integrated on chip and the manufacturer calibration data can be store on chip using a CMOS process with non-volatile memory (NVM). A truly single chip CNT sensor is feasible with the above integration.

5.2 Concluding Remarks

The feasibility of CNT-CMOS integrated sensor is demonstrated in this work. The CNT-CMOS integration is a novel idea and it is hoped that our study inspires further advances in this area such that CNT sensor system with smaller size, lower power consumption and better accuracy is developed.

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Publications related to this thesis

Journal Papers

Mandy LY Sin, **C. T. Chow**, Gary MK Wong, Wen J Li, Philip HW Leong, Ka Wai Wong, "Ultra-Low-Power Alcohol Vapor Sensors using Chemically Functionalized Multi-Walled Carbon Nanotubes," IEEE Transactions on Nanotechnology, May, 2007.

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Chun Tak Chow, Mandy L.Y. Sin, Philip H.W. Leong, Wen J. Li and K.P. Pun, "Design and Modeling of a CNT-CMOS Low-Power Sensor Chi," The 2nd Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, pages 1209-1214, Bangkok, Thailand, January 2007.

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Wenli Zhou, **C. T. Chow**, Wen J. Li, Philip Leong, "Carbon Nanotubes as Heating Elements for Micro-Bubble Generation", 2006 IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems, pages 1084-1087, Zhuhai, China, January 2006.

Appendix A

Schematic Diagram of ADC Testing

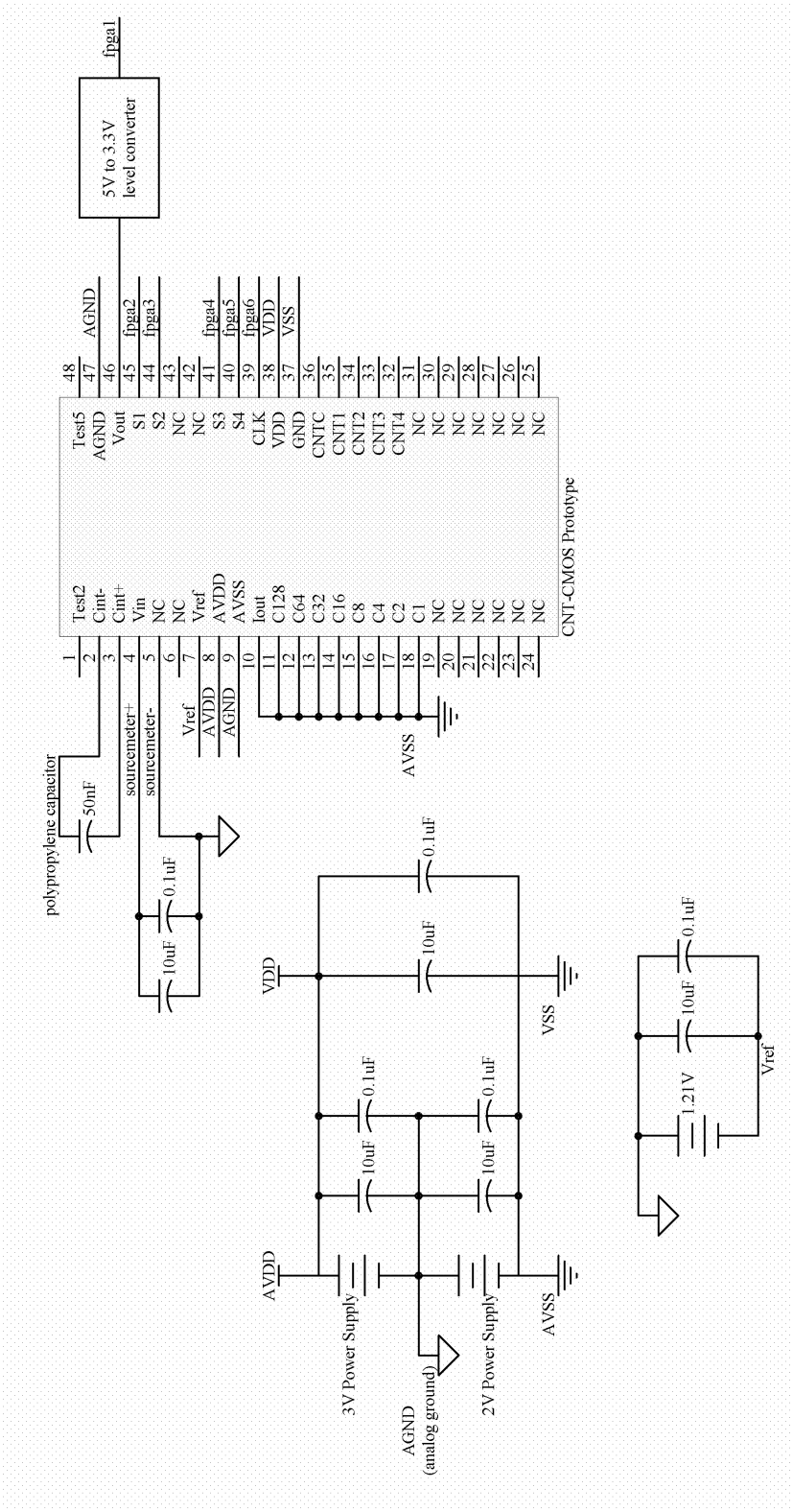

Figure A.1: Schematic Diagram of ADC Testing.